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DESIGN OF A 4 TIMES INTERLEAVED 2 KW AUTOMOTIVE DC-DC CONVERTER

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1 Introduction

With 48 V wiring systems becoming more common in automotive applications, especially for hybrid or more luxurious vehicles, the design of an efficient and small DC-DC converter that allows bi-directional power flow between the 48 V and the classical 12 V wiring system represents an important task.

Previous projects like [1] and [2] focus on optimizing an existing 1 kW DC-DC converter regarding its efficiency and power density. With this optimization completed, however, the goal of this project is the design of a new DC-DC converter with a power rating of 2 kW. The main focus point in that regard is a completely new design of the magnetic components, which should be as efficient, small and easy to integrate as possible. This extensive design process is shown in Chapter 2.

Furthermore, the new converter uses Silicon instead of Gallium Nitride technology for the power electronic switching devices. A reasoning for this choice as well as the selection of a suitable silicon switch is found in Chapter 3.

Having designed the magnetic components and chosen the switches, the arguably most important components of the DC-DC converter are specified, which allows additional auxiliary circuitry to be designed and the corresponding schematics to be created. This is described in Chapter 4, which additionally includes the PCB's layer stack-up. First considerations for the PCB layout are included as well, however, a complete layout design is out of the scope of this project. A 3D representation of the layout, including the inductor placement, can be seen in Figure 1.1.

The new converter also needs a new control hardware due to supply issues regarding the one chosen in [2]. The details of this as well as the selection of a new control hardware

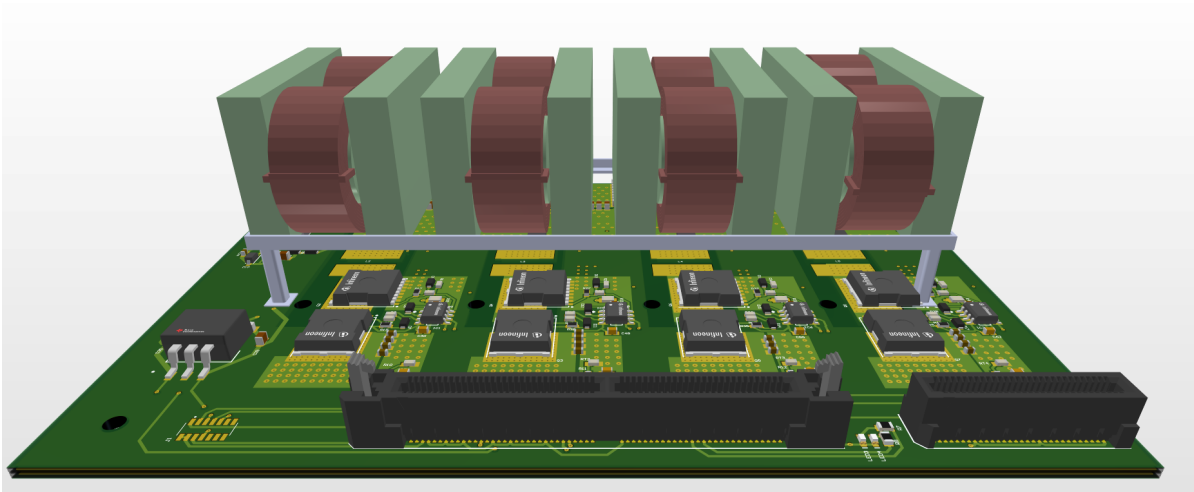


Figure 1.1: 3D representation of the converter PCB as well as inductor placement.

are described in Chapter 5.

Finally, in order to have a benchmark for future tests of this newly designed converter, the converter designed in [2] is built up during this project. However, due to some unexpected difficulties, it was not possible to test this converter in practice. The build up process as well as some of the encountered complications and their respective solutions are described in Chapter 6.

1.1 Project History

A brief summary of the project history for the bidirectional DC-DC converter is shown in Table 1.1. All these converters use gallium nitride transistors for the half-bridge switches of their four rails and have a rated power of 1 kW.

Pictures of these converters are shown in Figure 1.2. Note that, as mentioned previously, the converter of winter term 19/20 was not able to be fully built up and tested. Thus it is shown in Figure 1.2 only by its PCB in comparison to the summer term 19 converter's PCB.

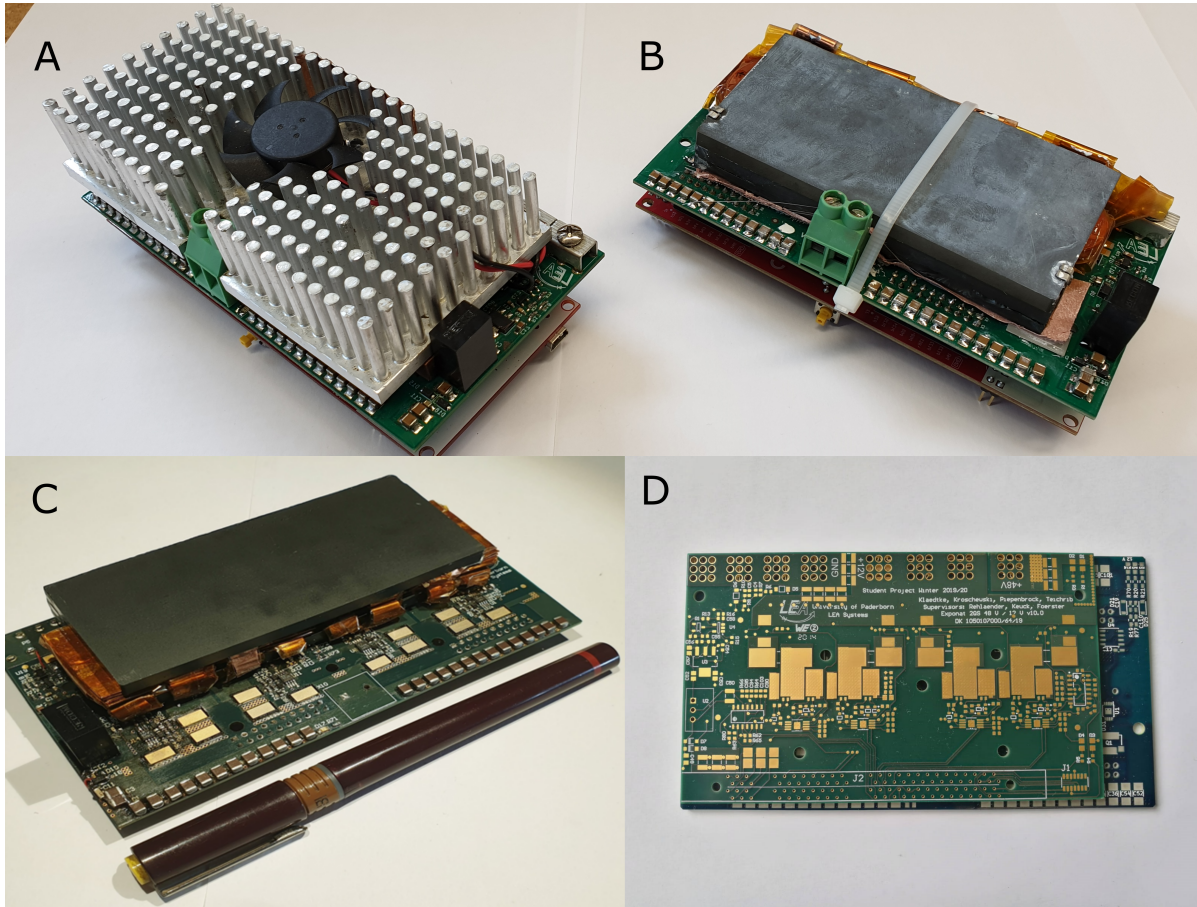


Figure 1.2: Converters of previous projects. (A) summer term 18, (B) winter term 18/19, (C) summer term 19, (D) winter term 19/20.

Title	Term	Focus	Control Hardware
Highly Compact, Efficient 48 V-12 V DC-DC Converter for Vehicle Electrical Systems	Summer 2018	Completely new design	F28379D Launchpad
Highly Compact, Efficient 48 V-12 V DC-DC Converter for Vehicle Electrical Systems with Coupled-Magnetics	Winter 2018/2019	Coupled magnetics for increased efficiency	F28379D Launchpad
Highly Compact, Efficient 48 V-12 V DC-DC Converter with Coupled-Magnetics in Watercooled Housing for Automotive Applications	Summer 2019	Housing design and integration	F28379D Launchpad
Redesign of a 1 kW Automotive DC-DC Converter for Increased Power Density	Winter 2019/2020	Compact redesign	F28335 Card

Table 1.1: Project history of the bidirectional DC-DC converter.

1.2 Bidirectional DC-DC Converter

This section roughly summarizes the basic operation principle of a bidirectional DC-DC converter. However, a more thorough explanation can be found in [3].

A simplified equivalent circuit diagram of the used topology is shown in Figure 1.3. The use of two transistors with anti-parallel (body-)diodes in a half bridge configuration allows this topology to conduct current of both negative or positive polarity, hence

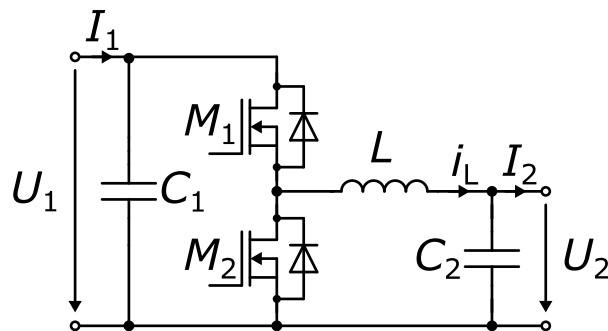


Figure 1.3: Equivalent circuit diagram of a bidirectional DC-DC converter.

being called bidirectional. The transistors M_1 and M_2 are switched alternately and, under idealized circumstances, the duty cycle

$$D = \frac{T_{\text{on}}}{T} = \frac{U_2}{U_1} = \frac{I_1}{I_2} \quad (1.1)$$

as a ratio of the switch-on time T_{on} of transistor M_1 to the switching period T determines the ratio of the input/output voltages U_1 , U_2 and currents I_1 , I_2 in steady state operation. The resulting inductor current waveform i_L has a triangular shape and is further discussed in Section 2.2.

2 Electromagnetic Field Simulations

While basic inductor design can be done by hand using simplified formulas, there are many nonlinear effects occurring that need to be dealt with in a different way. The use of FEM simulations allows to consider these nonlinearities and their effects on the electric and magnetic behavior of a magnetic component.

This chapter describes the design process of new magnetic components for the 2 kW converter, starting with the basic idea of a new topology with pairwise coupled coils. Since one of the design goals is a high efficiency and thus low losses, a theoretical basis of loss types occurring in magnetic components is given and it is shown how to properly consider these losses during FEM simulation.

Afterwards the concrete implementation of the theoretical loss analysis in the FEM tool ANSYS Maxwell (ANSYS Electronics Desktop 2018.2) is presented. The main focus is put on the modelling of losses, saturation and a parameterised geometry. To finally select a suitable core design, different topologies are compared in detail.

2.1 Magnetics Topology

A new aspect of the magnetic design that was not considered in earlier projects is the magnetic coupling of two separate inductors like it is shown in Figure 2.1. Assuming $\Phi_1 = \Phi_2$ this leads to full cancellation of magnetic flux in the now shared back conductor which can thus be removed without influencing the magnetic behavior. This new topology, however, essentially is a transformer and should be treated as such electrically,

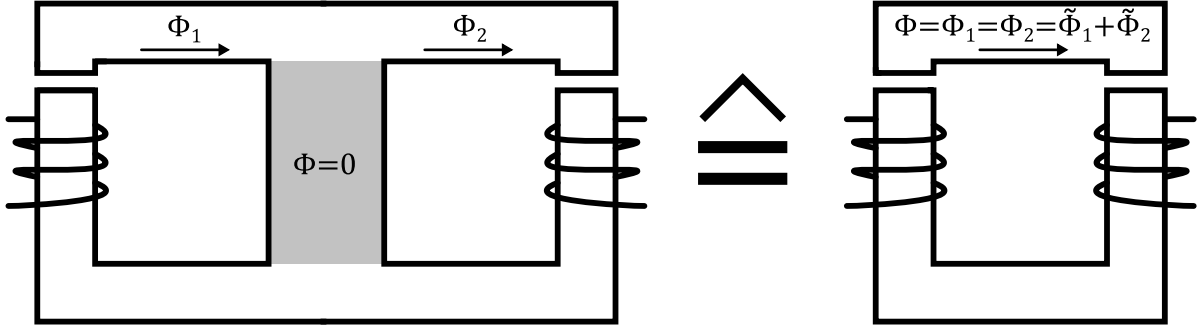


Figure 2.1: New Magnetic topology in which coupling the back conductors of two separate inductors leads to flux cancellation rendering the back conductors obsolete.

since the behavior shown in Figure 2.1 is only valid for perfect magnetic coupling of the coils.

The proposed circuit topology with these coupled inductors is shown in Figure 2.2. Like in previous projects, the four half bridges are switched with a phase shift of 90° to achieve current ripple cancellation at a duty cycle of $D = 0.25$ [1, p. 3]. It could be argued to use more half bridges than four to lighten the current load of each transistor but, based on the results in Chapter 3, this is not necessary and would also take up additional space on the PCB.

Switching both sides of the pairwise coupled inductors with a single half bridge leaves the two options to either connect both sides in series or parallel. Looking at Figure 2.1, a series connection of both windings essentially means doubling the number of turns N while also doubling the magnetic reluctance R_m and thus also doubling the total inductance $L \propto \frac{N^2}{R_m}$, which is also the standard result of connecting two non-coupled inductors in series. However, a series connection also doubles the resistance of the copper windings. So, while some of the loss types discussed in the following sections may decrease because of the lower current ripple that is gained by the increase in inductance, the DC ohmic losses would greatly increase. As shown in Subsection 2.7.3, this type of loss accounts for the majority of total losses for the analyzed magnetic topology. This is why a parallel connection of the coupled inductors like in Figure 2.2 is decided to be preferable, even though it decreases the total resulting inductance and thus increases

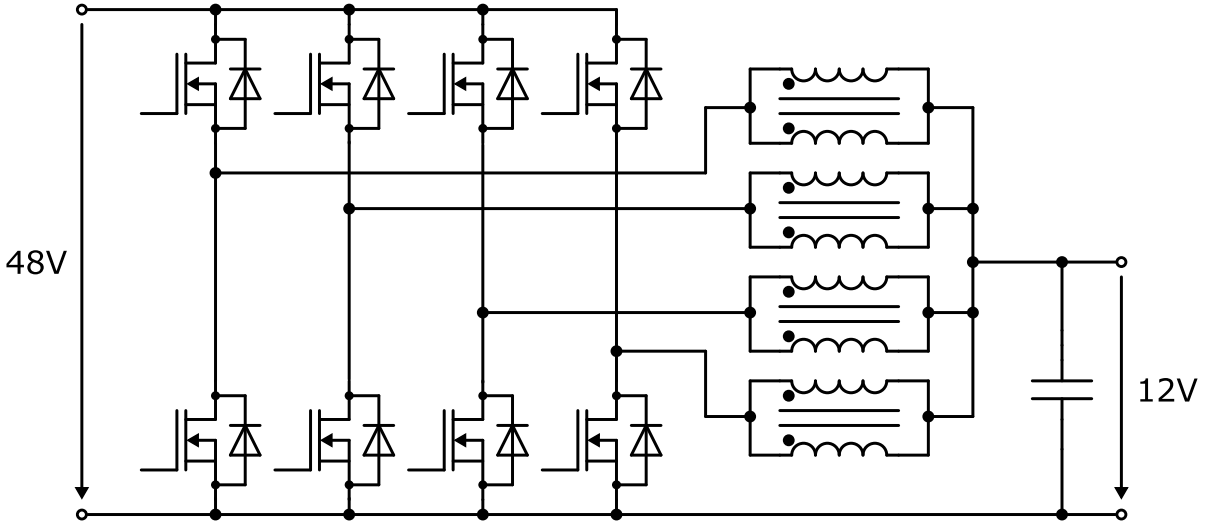


Figure 2.2: New proposed converter topology: Four times interleaved bidirectional DC-DC converter with coupled inductors.

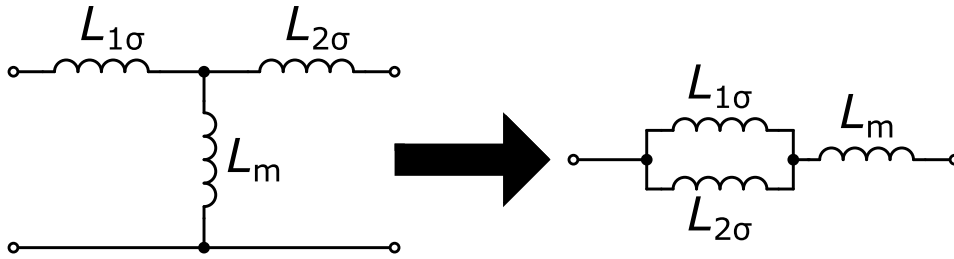


Figure 2.3: Simplified T-equivalent circuit of the transformer and resulting parallel connection.

the current ripple.

To derive the total resulting inductance for the parallel connection, the two coupled inductors are treated as a transformer which results the simplified equivalent circuit shown in Figure 2.3, where L_m is the mutual and $L_{1\sigma}, L_{2\sigma}$ are the stray inductances. The total inductance thus becomes

$$L = L_m + (L_{1\sigma} || L_{2\sigma}), \quad (2.1)$$

which can be simplified further under the following assumptions. By assuming the same

stray inductance $L_\sigma = L_{1\sigma} = L_{2\sigma}$ on both sides and thus defining the self inductance

$$L_1 = L_2 = L_m + L_\sigma, \quad (2.2)$$

on both sides, a single coupling coefficient k can be used to express the relation between self inductances, stray inductances and main inductance as

$$L_m = kL_1 = kL_2 \quad \text{and} \quad L_{1\sigma} = L_{2\sigma} = (1 - k)L_1 = (1 - k)L_2. \quad (2.3)$$

Using Equation 2.1 and Equation 2.3 the total inductance can thus be expressed as

$$\begin{aligned} L &= L_m + (L_{1\sigma} || L_{2\sigma}) = kL_1 + \frac{1}{2}(1 - k)L_1 \\ &= \frac{L_1}{2}(k + 1) = \frac{L_2}{2}(k + 1), \end{aligned} \quad (2.4)$$

which means that for perfect coupling ($k = 1$) the total inductance is as high as a single main inductance $L_{1/2}$ and for no coupling ($k = 0$) the total inductance is only half high. For perfect coupling, the total inductance compared to the self inductances does not decrease in this parallel connection, which may sound surprising. But looking at both sides of Figure 2.1, the self inductances of the right transformer are only approximately half as big as the two inductances on the left because the magnetic reluctance is twice as big on the right side, since it has two air gaps while keeping the same amount of turns as on the left.

To summarize, for a perfect coupling ($k = 1$) and a parallel connection of both (coupled) inductors, the two magnetic topologies shown in Figure 2.1 can actually yield the same total inductance while the right topology can save additional space by omitting a back conductor. This new magnetic topology is to be theoretically optimized in this project using numerical electromagnetic simulations and practically compared with already existing topologies once the converter is fully designed in future projects.

2.2 Loss Types

One very important result of a numerical electromagnetic simulation has to be an estimation of the losses caused due to non ideal behavior. The two types of losses occurring in the simulated magnetic components are ohmic losses, which are caused by current flowing through the copper windings, and core losses, which are caused by changes of the magnetic field in the ferrite core.

2.2.1 Ohmic Losses

With a triangular-shaped current signal, ohmic losses occur both due to the DC and the AC components of the signal. As a simplified approach, calculation of these losses can be done by assuming an equivalent series resistance R_{ESR} that is not dependent on the frequency of different AC signal components. In this case, the root mean square (RMS)

$$I_{\text{L,RMS}} = \sqrt{\frac{1}{T} \int_{t_0}^{t_0+T} i_{\text{L}}^2(t) dt} = \sqrt{I_{\text{L,DC}}^2 + \frac{1}{12} \Delta i_{\text{L}}^2} \quad (2.5)$$

of the triangular-shaped inductor current i_{L} with DC component $I_{\text{L,DC}}$, total ripple Δi_{L} and period T can be used to calculate the total ohmic losses

$$P_{\Omega} = I_{\text{L,RMS}}^2 R_{\text{ESR}}. \quad (2.6)$$

Due to additional effects that occur for AC inductor currents - such as eddy-currents, skin effects and proximity effects - Equation 2.6 is only an approximation of the total ohmic losses and gives less accurate results for signals with higher frequency components. However, these effects can be taken into account very precisely by using FEM simulation software.

By representing the inductor current and voltage using their respective fourier series

$$i_L(t) = I_{L,DC} + \sum_{n=1}^{\infty} \hat{i}_n \sin(2\pi nft + \alpha_n) \quad n \in \mathbb{N} \quad (2.7)$$

$$u_L(t) = U_{L,DC} + \sum_{m=1}^{\infty} \hat{u}_m \sin(2\pi mft + \beta_m) \quad m \in \mathbb{N} \quad (2.8)$$

with \hat{i}_n , α_n and \hat{u}_m , β_m respectively being the amplitude and phase shift of a current or voltage signal component at specific frequency $n \cdot f$ or $m \cdot f$, it can be shown according to [4, p. 109] that a more exact approach than Equation 2.6 can be rewritten as

$$P_{\Omega} = U_{L,DC}I_{L,DC} + \frac{1}{2} \sum_{n=1}^{\infty} \hat{u}_n \hat{i}_n \cos(\varphi_n) = P_{\Omega,DC} + \sum_{n=1}^{\infty} P_{\Omega,n} = P_{\Omega,DC} + P_{\Omega,AC}, \quad (2.9)$$

where $\varphi_n = \beta_n - \alpha_n$ is the lag of a current harmonic with respect to the voltage harmonic. This can be done because of the orthogonality relationship between the sine (or cosine) functions of different frequency components $m \neq n$ in Equation 2.7 and Equation 2.8. Thus follows that different frequency components do not interact with each other regarding the ohmic losses and that the losses $P_{\Omega,n}$ caused by each frequency component can be extracted individually from single-frequency AC simulations. To formally match Equation 2.9 and Equation 2.6, the equivalent series resistance can also be evaluated at each frequency $n \cdot f$ during the simulations. This yields

$$\begin{aligned} P_{\Omega} &= U_{L,DC}I_{L,DC} + \frac{1}{2} \sum_{n=1}^{\infty} \hat{u}_n \hat{i}_n \cos(\varphi_n) \\ &= I_{L,DC}^2 R_{ESR,DC} + \frac{1}{2} \sum_{n=1}^{\infty} \hat{i}_n^2 R_{ESR,n} \end{aligned} \quad (2.10)$$

where $R_{ESR,n}$ is a frequency dependent resistance that also takes into account the AC effects previously omitted in Equation 2.6.

The amplitudes \hat{i}_n and phase shift α_n can be derived by using a general representation of a T -periodic function $f(t)$ through its fourier series

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi nft) + b_n \sin(2\pi nft) \quad (2.11)$$

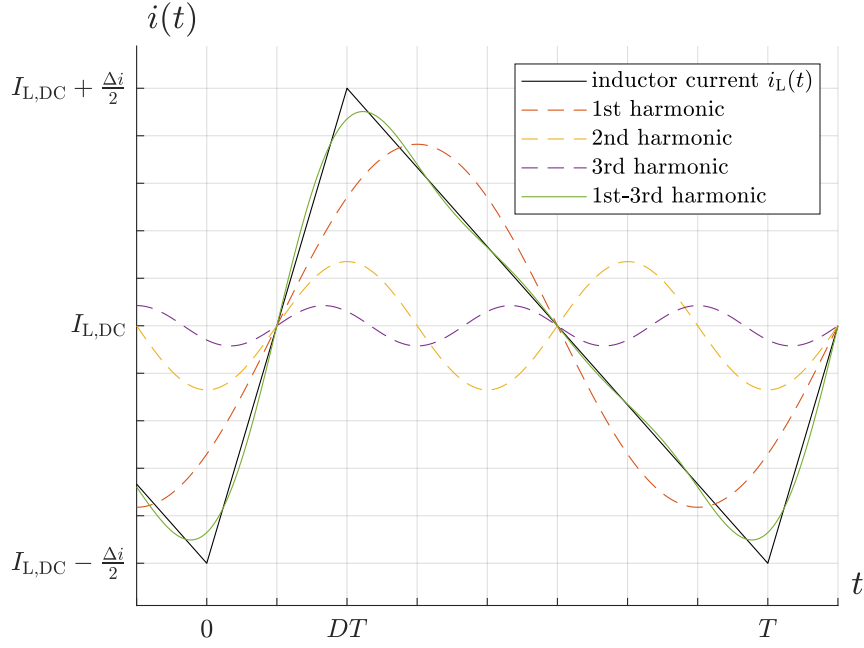


Figure 2.4: Triangular waveform of the inductor current i_L according to Equation 2.14 as well as first three harmonics and their sum according to Equation 2.15.

with the amplitudes

$$a_n = \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \cos(2\pi n f t) dt \quad n \in \mathbb{N}_0 \quad (2.12)$$

$$b_n = \frac{2}{T} \int_{t_0}^{t_0+T} f(t) \sin(2\pi n f t) dt \quad n \in \mathbb{N}_0, \quad (2.13)$$

which always yields $b_0 = 0$. Using the duty cycle D to define the inductor current as

$$i_L(t) = I_{L,DC} + \begin{cases} \frac{\Delta i}{DT} t & , t \in [-\frac{DT}{2}, \frac{DT}{2}] \\ \frac{\Delta i}{2} - \frac{\Delta i}{(1-D)T} (t - \frac{DT}{2}) & , t \in [\frac{DT}{2}, T - \frac{DT}{2}] \end{cases}, \quad (2.14)$$

it can be seen from Figure 2.4 that $i_L(t)$ is an odd signal, which yields the DC component $a_0 = I_{L,DC}$ and no other amplitudes of even components $a_n = 0 \forall n \in \mathbb{N}$. This also means $\hat{i}_n = b_n$ and $\alpha_n = 0$ in context of Equation 2.7. The remaining amplitudes \hat{i}_n can thus

be calculated using Equation 2.12 and Equation 2.13 which yields

$$\hat{i}_n = \frac{\Delta i}{n^2 \pi^2 D (1 - D)} \sin(n\pi D). \quad (2.15)$$

Since $P_{\Omega,n} \propto \hat{i}_n^2 \propto \frac{\sin(n\pi D)}{n^4}$, only low order harmonics are relevant to the ohmic losses. Also because the converter is designed to operate at $D = 0.25$ under ideal circumstances, harmonics with an order $n = 4m$, $m \in \mathbb{N}$ have an amplitude $\hat{i}_n^2 = 0$. For these two reasons only harmonics up to third order are considered in the simulation for ohmic losses.

2.2.2 Core Losses

Losses in the core material of an inductor mainly occur due to effects such as hysteresis and eddy-currents which are caused by changes in the magnetic field. Although the DC component of the magnetic field still has an influence on the losses by shifting the operating point on the magnetization curve, it is disregarded in this analysis because it is usually very hard to model in simulations with the data given by core manufacturers.

Since some of the loss mechanisms in magnetic material cannot be described very well analytically, a widely used alternative are empirical equations that describe the power loss density P_v like Steinmetz's equation

$$P_v = k f^a \hat{B}^b \quad (2.16)$$

for sinusoidal magnetic flux density waveform with frequency f and amplitude \hat{B} or the improved generalized Steinmetz equation (iGSE)

$$P_{v,iGSE} = \frac{1}{T} \int_{t_0}^{t_0+T} k_i \left| \frac{dB}{dt} \right|^a \Delta B^{b-a} dt \quad (2.17)$$

with

$$k_i = \frac{k}{(2\pi)^{a-1} \int_0^{2\pi} |\cos \theta|^a 2^{b-a} d\theta} \quad (2.18)$$

for any magnetic flux density waveform $B(t)$. The Steinmetz parameters a , b and k can be estimated using Equation 2.16 with empirical data given by the core manufacturer. Because the inductor current has a triangular-shaped waveform in steady state, the resulting magnetic flux density waveform is not sinusoidal which means that the iGSE should be used.

Since simulation of time-domain signals in ANSYS Maxwell takes too long for an iterative optimization process and the eddy current solver can only calculate core losses using Steinmetz' equation for single frequencies, the work of [5] exports simulation data for the first three harmonics of the magnetic flux density and uses that data to recreate the triangular-shaped time-domain signal and then use the iGSE. This approach however is still very time consuming and also vulnerable to manual errors.

An easier approximation of the core losses can be made by assuming that the inductor current shown in Equation 2.14 produces a similar triangular-shaped magnetic flux density waveform

$$B(t) = B_{\text{DC}} + \begin{cases} \frac{\Delta B}{DT}t & , t \in [-\frac{DT}{2}, \frac{DT}{2}] \\ \frac{\Delta B}{2} - \frac{\Delta B}{(1-D)T}(t - \frac{DT}{2}) & , t \in [\frac{DT}{2}, T - \frac{DT}{2}] \end{cases}, \quad (2.19)$$

where B_{DC} and ΔB can vary throughout the core. This assumption should be valid if nonlinear effects are omitted and the core material is behaving approximately frequency independent in the frequency range of the three relevant harmonics mentioned in Subsection 2.2.1. In the simulation, ΔB is constant and $\frac{dB}{dt}$ piecewise constant (for every volume element) in steady state, which means that the iGSE can be simplified to

$$P_{v,\text{iGSE}} = kf^a \hat{B}^b \frac{2(D^{1-a} + (1-D)^{1-a})}{\pi^{a-1} \int_0^{2\pi} |\cos \theta|^a d\theta} = kf^a \hat{B}^b g(a, D) \quad (2.20)$$

with $\hat{B} = \frac{\Delta B}{2}$. Comparing Equation 2.20 to Equation 2.16 shows that the structure of the iGSE for this triangular-shaped waveform perfectly matches the original Steinmetz' equation except for a factor $g(a, D)$ that is only dependent on the duty cycle D and one of the Steinmetz parameters a which is shown in Figure 2.5. This means the core losses can be approximated with a single frequency sinusoidal simulation and using the

$P_{\text{loss}} \backslash \begin{matrix} B \\ f \end{matrix}$	25 mT	50 mT	100 mT	200 mT	300 mT
50 kHz	-	5.5 kW/m ³	27.8 kW/m ³	141.7 kW/m ³	377.5 kW/m ³
100 kHz	2.9 kW/m ³	13.3 kW/m ³	68.6 kW/m ³	364.7 kW/m ³	-
200 kHz	7.5 kW/m ³	39 kW/m ³	199.5 kW/m ³	1112.3 kW/m ³	-
300 kHz	15.4 kW/m ³	80.4 kW/m ³	414.5 kW/m ³	2199.2 kW/m ³	-

Table 2.1: Manufacturer's loss density values (TDK N95 at 25 °C) [6]

integrated core loss model in ANSYS Maxwell if the factor $g(a, D)$ is considered.

Notably, for a steady state duty cycle $D = 0.25$ and the Steinmetz parameter $a = 1.5$, which is close to the actual parameter estimated in Section 2.3, the approximation factor yields $g(a = 1.5, D = 0.25) \approx 1.018$. This means the chosen approximation is actually very close even if the factor would be disregarded. However, in Figure 2.5 it can also be seen that this is only the case for certain duty cycles and Steinmetz parameters, so it should still be checked carefully before an approximation like this is made.

Furthermore, depending on the distribution of flux density B throughout the core, the estimated Steinmetz parameters can change if they are locally estimated around a given flux density. This, however, is only relevant if the amplitude of the magnetic flux density \hat{B} varies significantly throughout the core, which is not the case as can be seen in Subsection 2.7.3.

2.3 Core Loss Model in ANSYS Maxwell

According to the theoretical illustrations of the core losses in Subsection 2.2.2 for an FEM simulation a material has to be defined which fits the real behavior in an adequate way. Taking the given loss density values from the core material's manufacturer, a specific core loss model can be implemented in ANSYS Maxwell by creating a user defined material. For that purpose curves of the loss density and the magnetic flux density for fixed frequencies can be drawn out of Table 2.1. The program automatically calculates Steinmetz-parameters from the provided data. Both, curves and Steinmetz-parameters

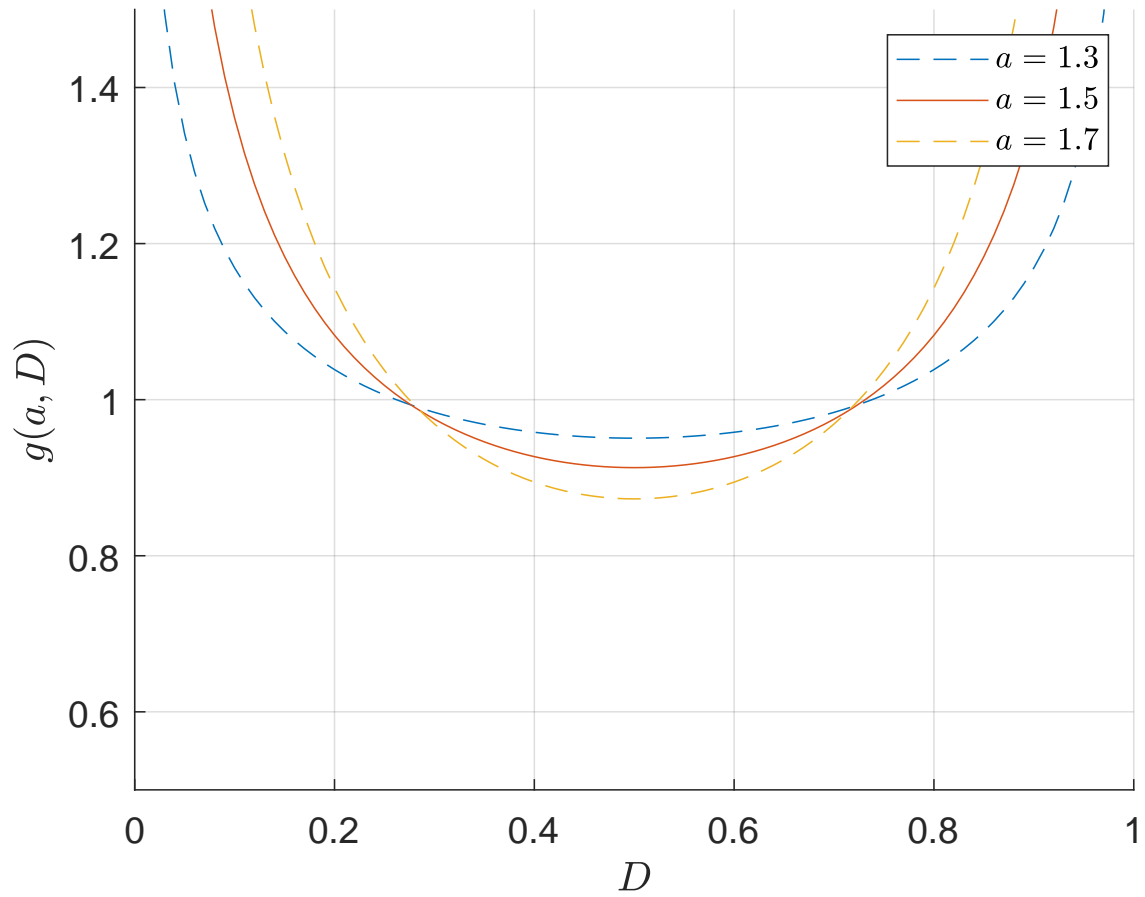


Figure 2.5: Approximation factor $g(a, D)$ for different Steinmetz parameters a and duty cycles D . The case $a = 1.5$ is very close to the actual estimation seen in Section 2.3.

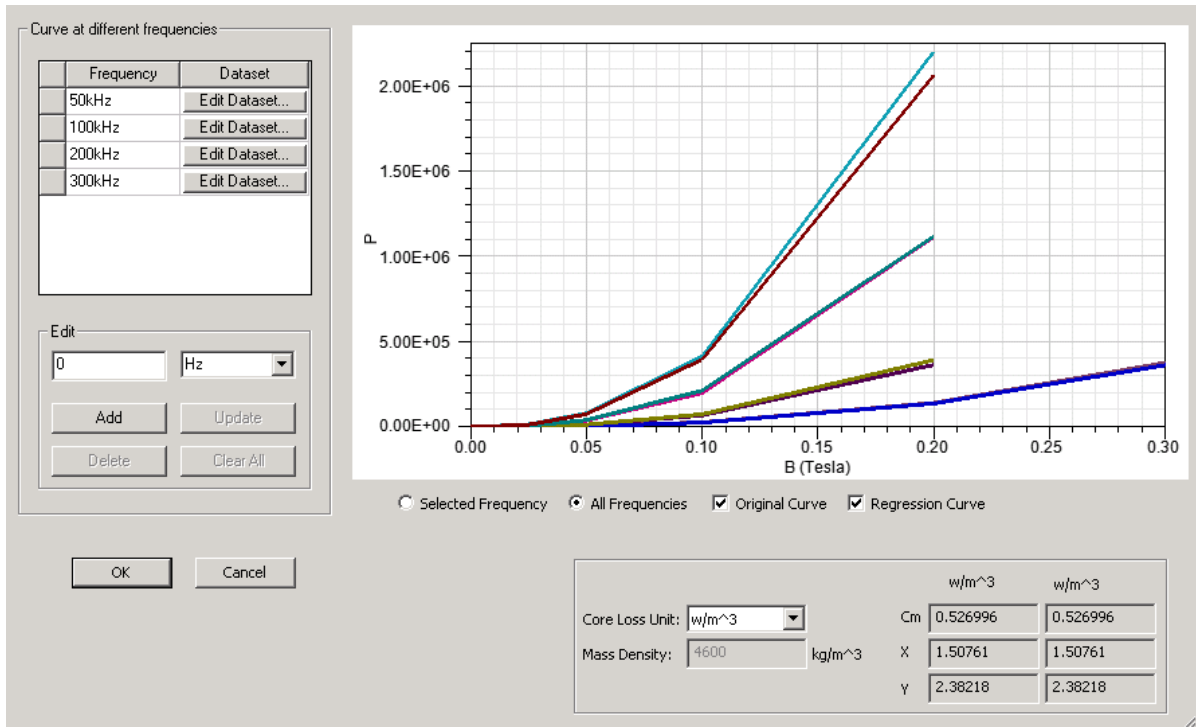


Figure 2.6: Core loss model in ANSYS

can be seen in Figure 2.6. The coefficients correspond to Equation 2.16 by replacing $\{k, a, b\}$ with $\{C_m, X, Y\}$. As the switching frequency for the case of maximum power has been stated as 100 kHz, the curves for the first three harmonics are covered with the underlying data. This procedure allows a comfortable way of estimating core losses in the post processing of a simulation.

To proof the accuracy of this method, a control simulation with the edited material is to be performed. In the manufacturer's data sheet the relative core losses measured on R34 toroid cores are given. These shall be compared to a simulation on a CAD model of this core geometry with the defined material. Instead of presenting the whole simulation, only the essential criteria of proof shall be taken into account. As a parameter sweep for the exciting currents shows, in a double logarithmic scale the relation of the current and the loss density equals a straight line. Further, underlying to operate in a non saturated operation point, it holds that the exciting current is directly proportional to the magnetic flux density. With that information the power loss density can be plotted

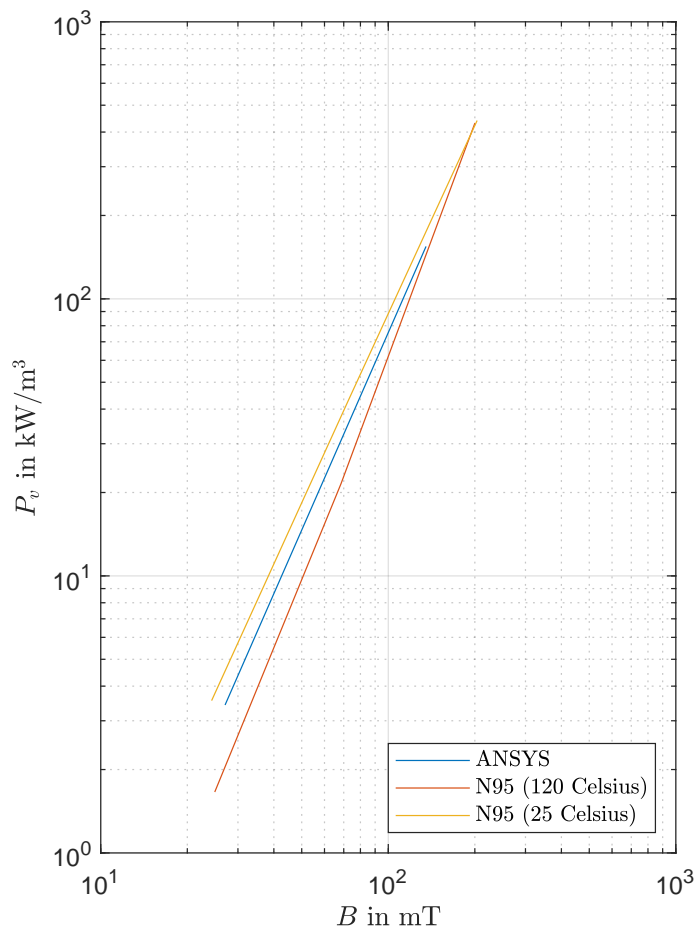


Figure 2.7: Loss density of TDK N95 core material on an R34 toroid core [6]

above the magnetic flux density by only two data points which are taken as probes out of the simulation results. [6]

As Figure 2.7 shows, the loss characteristic from the data sheet corresponds to the results of the toroid simulation in ANSYS. The loss characteristic of the toroid simulation in ANSYS stated between the operation points of 25 °C and 120 °C. As the temperature of the liquid cooling system in automotive applications is assumed to be 60 °C this assumption seems to be valid, but is no longer part of the projects investigations.

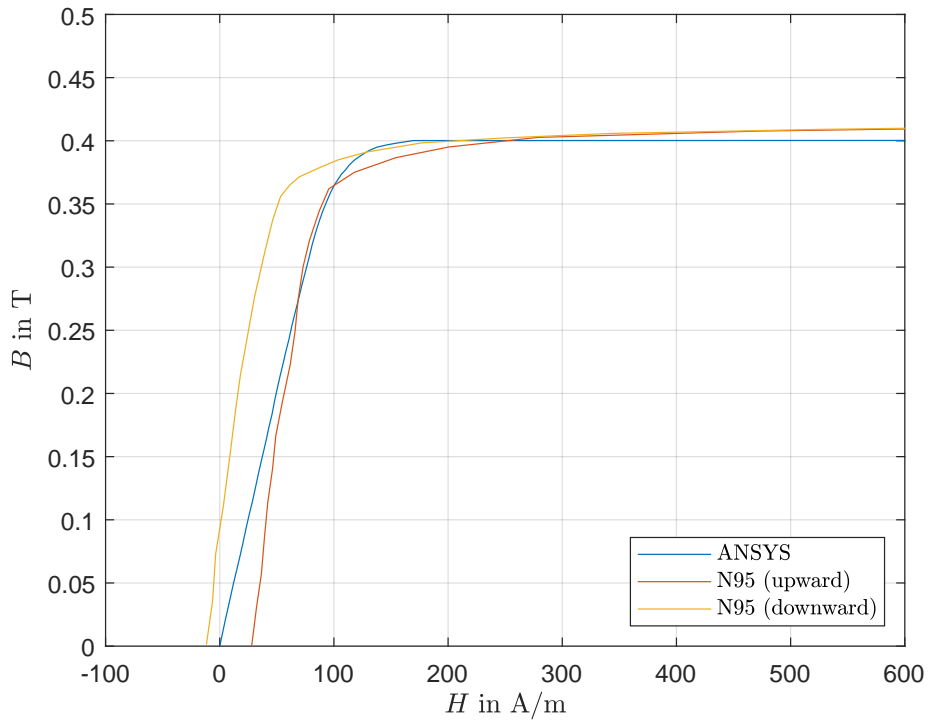


Figure 2.8: Magnetization curves (Comparison of the N95 data sheet values with the saturation model in ANSYS)

2.4 Saturation in ANSYS Maxwell

Another effect, that has to be considered, in terms of setting up the core material for an FEM simulation is the saturation. As non idealized core materials do not behave in a linear way, for high magnetic flux densities the permeability gets close to the vacuum permeability. To model this effect in the core material, a magnetization curve (in terms of a B-H curve) may be added. As Figure 2.8 shows, in ANSYS the magnetization curve is only implemented with one curve which equals the initial magnetization curve. The hysteresis effects due to an upward and downward curve are not modeled here. These effects are summed up in the previously explained core loss model. The idea of separating those very related physical effects is related to enable a much more efficient way of computing.

Next to the solved question of modelling the effects of saturation, there must also be

a metric of estimating, how much the core is saturated during a certain simulation run. In this project the very simple approach of evaluating the mean value of the magnetic flux density through one of the ferrite-tablets in the inner part of the windings at the maximal current is applied. Then afterwards a comparison with the magnetization curve allows conclusions about the status of saturation.

Another discussed, but due to the higher effort finally not used, approach is to evaluate the sloping inductance values for a wide applied current range. When the desired maximal current is reached, the degree of saturation can be determined.

2.5 CAD-Model of the Coil

To perform simulations with the FEM, a suitable CAD model is needed. There are certain requirements for the model, that have to be taken into account during its development. All parts of the geometry that are used for current conduction must either be of a closed loop form or end and begin perfectly matched on the so called 'Region' which defines the boundary of the three dimensional computing area. As one discussed way of building up the windings is shown in Figure 2.9, a back-conductor has to be placed between the most inner and outer winding. A more easy approach is to use the predefined 'TransCoil' model which can easily shift between a vertical and horizontal winding style. Also, it has to be found a compromise between exact modelling and leaving out unnecessary details. To enable a high flexibility in changing the whole geometry the model has to be fully defined by variable parameters. Within this dynamic modelling, changes of the components' dimensions like the width of the ferrite core or the thickness of the foil windings can be modified by only changing the variable values. Also changes that effect the whole model, like the number of turns or the air gap, can be edited without any changes in the basic model. For that purpose, several independent and some more dependent geometric parameters are defined. On one hand this means a very mutable customization of the geometry, on the other hand this means a lot of degrees of freedom in finding an optimal solution.

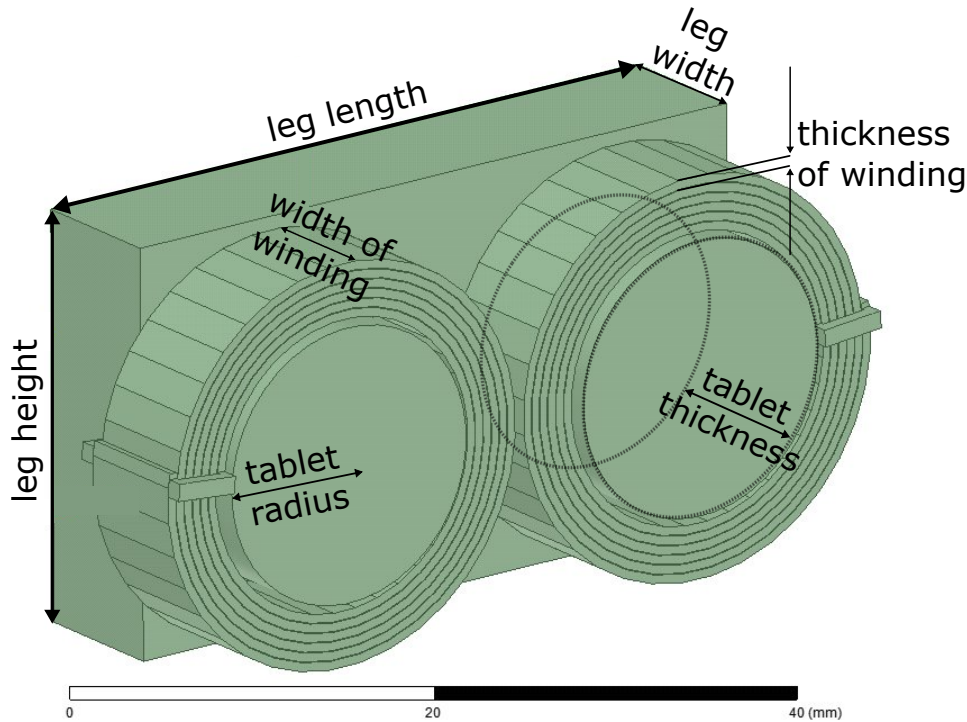


Figure 2.9: Parametric CAD model in ANSYS

2.6 Remarks on the FEM-Simulation

As already started in Section 2.5 the optimization of the coil's geometric parameters does not seem to be very trivial. First of all the high flexibility of several degrees of freedom opens a wide feature space. Although course modern FEM servers enable fast calculations, one simulation run for this project takes some minutes. On the LEA FEM server one single simulation run takes from 5 to 20 minutes depending on accuracy in terms of meshing effort and maximal energy error. This combination ends for a practicable optimization algorithm in a long computation time. Even more problematic is the setup of a suitable cost function. As especially in terms of the automotive environment crucial criteria are the efficiency and the required space. Of course both quantities can be taken into account for an optimization. But a weighting in terms of comparing the importance of space and efficiency seems obviously, as both quantities have different units, not very rational.

If one discusses only optimizing the quantity of power loss (which is in this project the same as optimizing efficiency), a huge geometry will be the result as the losses decrease with bigger widths of the windings and cores. Because of the simultaneously developed PCB layout a maximal width of the winding's geometry can be assumed as given. So that the external dimensions of the geometry are more or less fixed. Also, the two variables 'leg height' and 'leg width' should be chosen to yield the same cross sectional area as the 'tablet radius'. This assumption obviously makes sense as the degree of saturation should be chosen the same in the core's 'tablets' and 'legs' and is due to its defined metric from Section 2.4 proportional to the cross sectional area. But even with these assumptions and simplifications only the power loss of the magnetic component is to be optimized. For a global loss optimization also the losses due to non ideal behavior of the electrical components, especially the MOSFETs, have to be taken into account.

As the whole system considering the several non ideal effects, cannot be easily described by a linear problem it is practically impossible to find or ensure one point as the global optimum.[7] Because of that and in terms of time management due to the required effort it was decided to do a more practical orientated way of finding a configuration of the magnetics. Maybe for future student groups the done preliminary work can be useful to develop a more general approach of optimization.

2.6.1 Simulation-Workflow

To figure out the needed quantities for the theoretically described ohmic and core losses as well as the status of saturation in total two static and four eddy current simulations have to be performed for each geometric configuration.

At first one static simulation is carried out with the peak current value, to figure out whether the core is in saturation or not. A second static simulation needs to be done to evaluate the ohmic losses due to the DC part of the inductor-current. Of course both simulations can be done at once by a parameter-sweep, which saves computational effort as the mesh can be reused. Problematic for the simulation of the peak current value is, that the inductivity must be known in advance to calculate the peak current value.

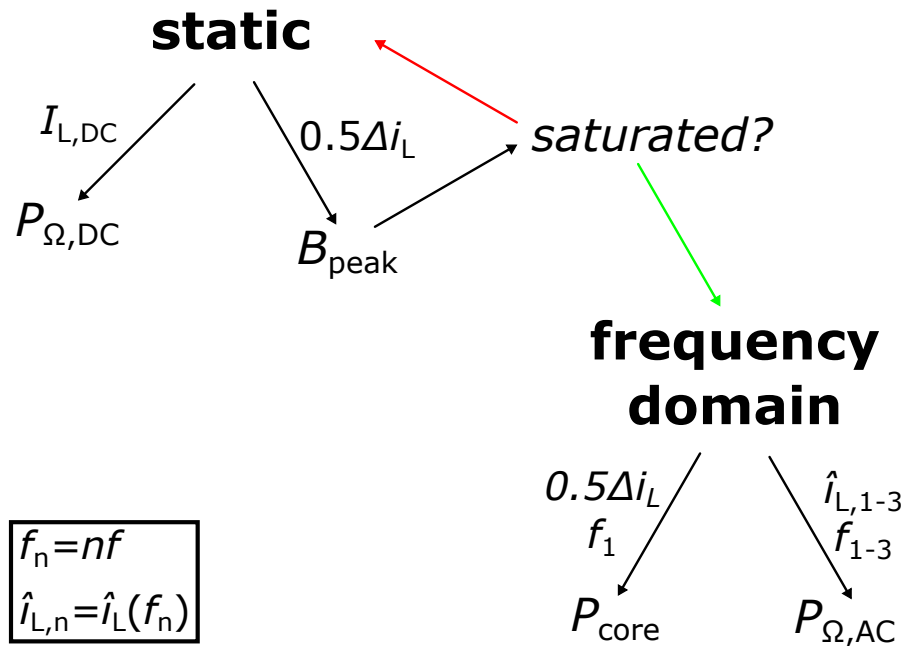


Figure 2.10: Simulation workflow

With an eddy current solver then two simulations are to be performed at the switching frequency which is stated to be the fundamental frequency. For the core loss evaluation one simulation at the fundamental frequency must be carried out with an excitation current amplitude half of the current ripple. For the ohmic losses due to eddy current effects, caused by the AC part of the inductor-current, the second simulation at the switching frequency must be simulated with the corresponding Fourier coefficient. The analogous procedure must be run for the second and third harmonic frequency with the associated Fourier coefficients for the current.

2.7 Simulation Results

To complete the FEM simulation one variant of the inductor shall be found. For that purpose two different types of windings are compared and one of this types is then optimized by iterating a fixed operation point.

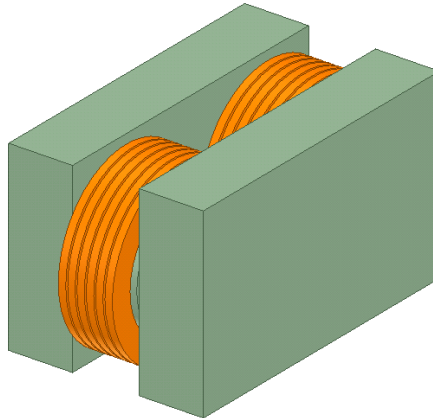


Figure 2.11: CAD model of the vertical winding approach

2.7.1 Comparison of Winding Types

There are two main topologies in the way of building up windings by copper sheet. They can either be assembled horizontally or vertically based on the ferrite tablet.

The horizontal approach can easily be produced by wrapping up one isolated copper band and lead out the inner end by folding or soldering in a 90° angle.

The vertical approach (Figure 2.11), which is used in the converter from the winter term 19/20, consists of many individual parts of copper sheet. These parts have to be cut out and soldered together separately. This procedure is not only time-consuming, but also wastes a lot of copper. In an industrial context this means that such a manufacturing process is much more cost-intensive.

A comparison of both techniques shall indicate, whether it is worth putting the extra effort into producing the vertical approach of windings. For a general comparison one must compare both topologies in their optimal configuration. As stated before, practically it is nearly impossible to find the optimal global choice of parameters. As a claim for this concrete project two same sized approaches in terms of outer dimensions shall be compared with each other. As it can be seen in Table 2.2 the 'vertical' approach cannot be called better than the 'horizontal'.

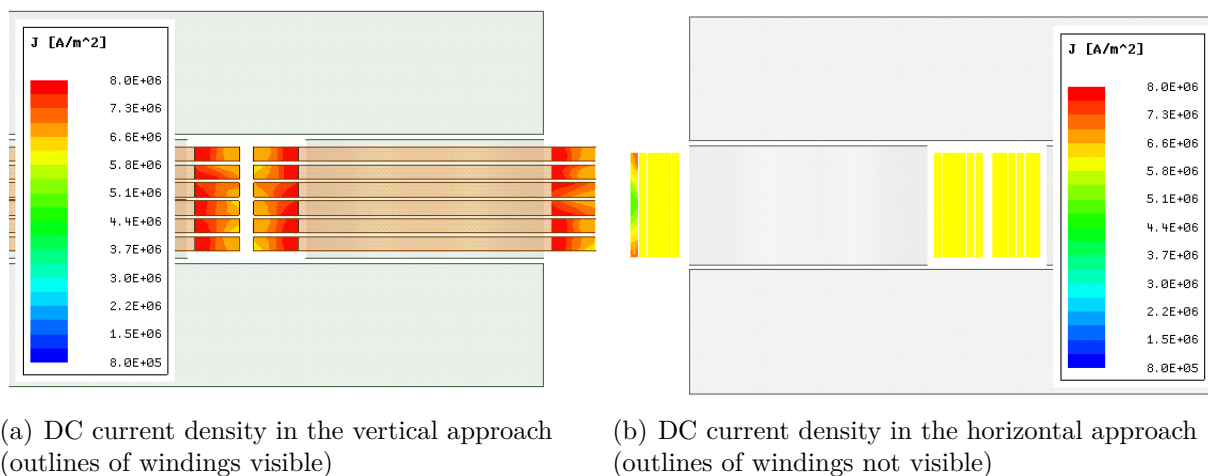


Figure 2.12: Distribution of the magnitude of the DC current densities in vertical and horizontal windings

In Table 2.2 the results of both approaches are summed up labeled as run '*vert.*' and '*hor.*'. It shows out, that the vertical approach effects a slightly higher self inductance value, although the number of turns and the ferrite core is the same.

However, the horizontal variant in total has slightly lower losses. Especially the ohmic losses contributed by the DC current are lower for the horizontal approach. This can be explained by the lower cross section of 2.88 mm^2 for the horizontal approach compared to 3.5 mm^2 for the vertical winding. The built up of the vertical windings (Chapter 6) shows that soldering the single copper pieces leads to a slightly higher distance between the turns. This again effects a lower fill factor compared to the easily wound up foil windings.

A closer view on the distribution of the current density of both topologies is shown in Figure 2.15. For both field distributions the same range of the current densities' magnitudes is predefined. Figure 2.12(a) shows for the vertical approach that the part of each winding which is close to the core has a higher magnitude of current density than the outer one. That is why effectively not the full cross section is used for the current conduction. Whereas Figure 2.12(b) does not show this effect for the horizontal approach due to the less radial extension of every single winding. The only deviation of the current density on the very left side of the right figure is contributed by the necessary

Run	B_{mean}^*	$P_{\Omega,DC}$	$P_{\Omega,AC}$	P_{core}	P_{total}	Inductance**
<i>vert.</i>	322 mT	2.00 W	0.86 W	0.22 W	3.08 W	9.18 μH
<i>hor.</i>	326 mT	1.72 W	0.84 W	0.31 W	2.87 W	8.62 μH

* B_{mean} is the mean mag. flux density through the centered cross section of the ferrite tablet

**Inductance in this context means the respective self inductance

Table 2.2: Results of the compared winding topologies

Run	turns	tablet radius	tablet thickness	leg height	leg width	air gap
<i>vert.</i>	6	8 mm	8 mm	24 mm	8.3 mm	0.35 mm
<i>hor.</i>	6	8 mm	8 mm	24 mm	8.3 mm	0.35 mm

Table 2.3: Parametric configuration the presented winding topologies

back-conductor which is explained in Section 2.5.

All in all it does not seem, that any variant means a technological advantage in general. With the above stated explanations regarding the more demanding built up of the vertical variant, from now on only the horizontal approach is to be investigated.

2.7.2 Iteration of an Operation Point

Due to the results of the topologies' comparison further only the horizontal approach shown in Figure 2.9 is to be investigated. Since a global optimization is practically not feasible, some assumptions are made. The total width of one rail is fixed to max. 26.7 mm due to the PCB layout. In addition to that the height of the ferrite legs should not exceed the diameter of the outer winding, since this creates unused space. Of course in this project's application there is some free space above the inductor and an imaginary cubic box around the converter. But as for industrial purposes instead of an evaluation board a micro controller is directly placed on the PCB this can be taken as a reasonable assumption. Finally the leg height is assumed to be 25 mm.

In addition to these geometric boundary conditions an inductance value of about 9.6 μH is desired, corresponding to the assumed value for the switch selection in ??.

Also, a mean magnetic flux density through the centered cross section of the ferrite tablet of about 320 mT should not be exceeded. This value means a 20 % safety margin towards a full saturation referring on Figure 2.8. For this operation point various parametric compositions are simulated and their losses shall be compared. Due to the strict parametric coupling of the ferrite tablet and the outer legs, for every number of turns only one variation of parameters remains. The parametric configurations are presented in Table 2.5 as well as the simulations' results are summed up in Table 2.4. To make the text more readable, the compared parametric configurations of the investigated horizontal windings are enumerated from 'a' to 'f' referring on Table 2.5.

As run 'a' shows, with five turns it is nearly impossible to reach the desired inductance but keeping the size of the geometry such small under the assumption of not getting into saturation. This can be clearly explained due to the very tight winding, that occurs in a high ohmic resistance. For this reason configurations with five or less turns are no longer point of investigation. Vice versa run 'f' shows, that ten or more windings are also not suitable for this application as the losses increase with that high number of turns.

For all variations from six to nine turns it is easily possible to achieve the desired inductance value and keep the core's flux density below the limit of saturation. For this specific parametrization it shows out, that a higher amount of turns decreases the ohmic losses due to the DC current. At first sight this seems to be a little counter intuitive, but as Table 2.5 shows, the extended current path is compensated by an increased winding width.

The ohmic losses due to the AC current on the other hand increase with the number of turns. This can be explained by a view on the distribution of the current density's magnitude across one winding, which is shown in Figure 2.13. It shows out that the current density is very high in the most inner winding, but also that the current density of all windings is concentrated on the margins. Obviously this means, that not the whole cross section is used for the current conduction. As a result of this, it turns out that the increased winding width no longer compensates the extended current path due to a higher amount of turns.

The effect of concentrated current densities close to the air gaps can be explained

Run	B_{mean}^*	$P_{\Omega,\text{DC}}$	$P_{\Omega,\text{AC}}$	P_{core}	P_{total}	Inductance**
<i>a</i>	319 mT	2.68 W	0.56 W	0.33 W	3.57 W	9.25 μH
<i>b</i>	319 mT	1.80 W	0.71 W	0.27 W	2.79 W	9.60 μH
<i>c</i>	318 mT	1.61 W	0.94 W	0.22 W	2.78 W	9.67 μH
<i>d</i>	309 mT	1.48 W	1.07 W	0.19 W	2.73 W	9.56 μH
<i>e</i>	323 mT	1.37 W	1.27 W	0.17 W	2.81 W	9.59 μH
<i>f</i>	322 mT	1.41 W	1.38 W	0.15 W	2.93 W	9.75 μH

* B_{mean} is the mean mag. flux density through the centered cross section of the ferrite tablet

**Inductance in this context means the respective self inductance

Table 2.4: Results of the FEM Simulation

Run	turns	winding width	winding thickness	tablet radius	tablet thickness	leg height	leg width	air gap
<i>a</i>	5	4 mm	0.5 mm	9.17 mm	5 mm	25 mm	10.60 mm	0.28 mm
<i>b</i>	6	7 mm	0.5 mm	8.50 mm	8 mm	25 mm	9.08 mm	0.35 mm
<i>c</i>	7	9 mm	0.5 mm	7.94 mm	10 mm	25 mm	7.91 mm	0.44 mm
<i>d</i>	8	11 mm	0.5 mm	7.36 mm	12 mm	25 mm	6.81 mm	0.54 mm
<i>e</i>	9	13 mm	0.5 mm	6.75 mm	14 mm	25 mm	5.73 mm	0.62 mm
<i>f</i>	10	14 mm	0.5 mm	6.37 mm	15 mm	25 mm	5.11 mm	0.74 mm

Table 2.5: Parametric configuration of presented runs

The green marked line represents the final coil configuration.

by the magnetic field density which is shown in Figure 2.14. It can be seen, that the magnetic flux the magnetic flux spreads into the interior space and penetrates the copper foils. Due to the induction law additional currents are induced in each winding. Exactly these induced currents can be seen in Figure 2.13. For this reason in the CAD model the copper width of winding is considered to be 1 mm lesser than the thickness of the ferrite tablet. A deeper investigation of the spreading effects is not performed in this project.

2.7.3 Final Coil Configuration

The configuration with the number of eight turns in total has the lowest losses, operates below saturation and provides a good inductance. Out of the theoretical simulation

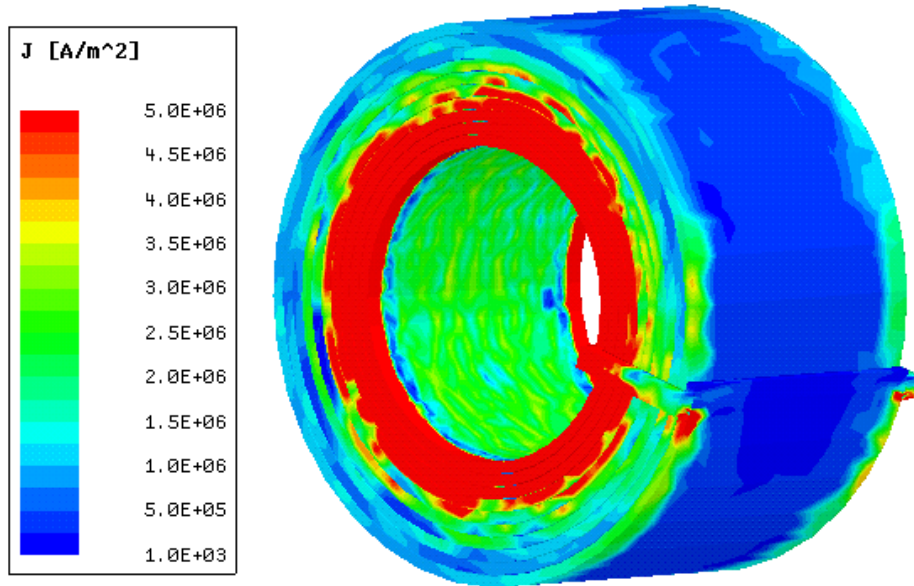


Figure 2.13: Current density for a sinusoidal current at 100 kHz and 10 turns (logarithmic representation)

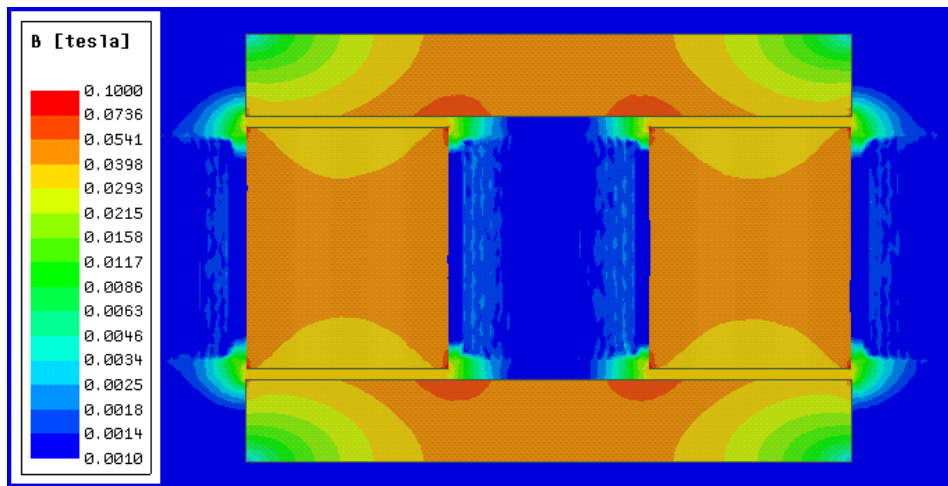


Figure 2.14: Magnetic field density for a sinusoidal current at 100 kHz and 10 turns (logarithmic representation)

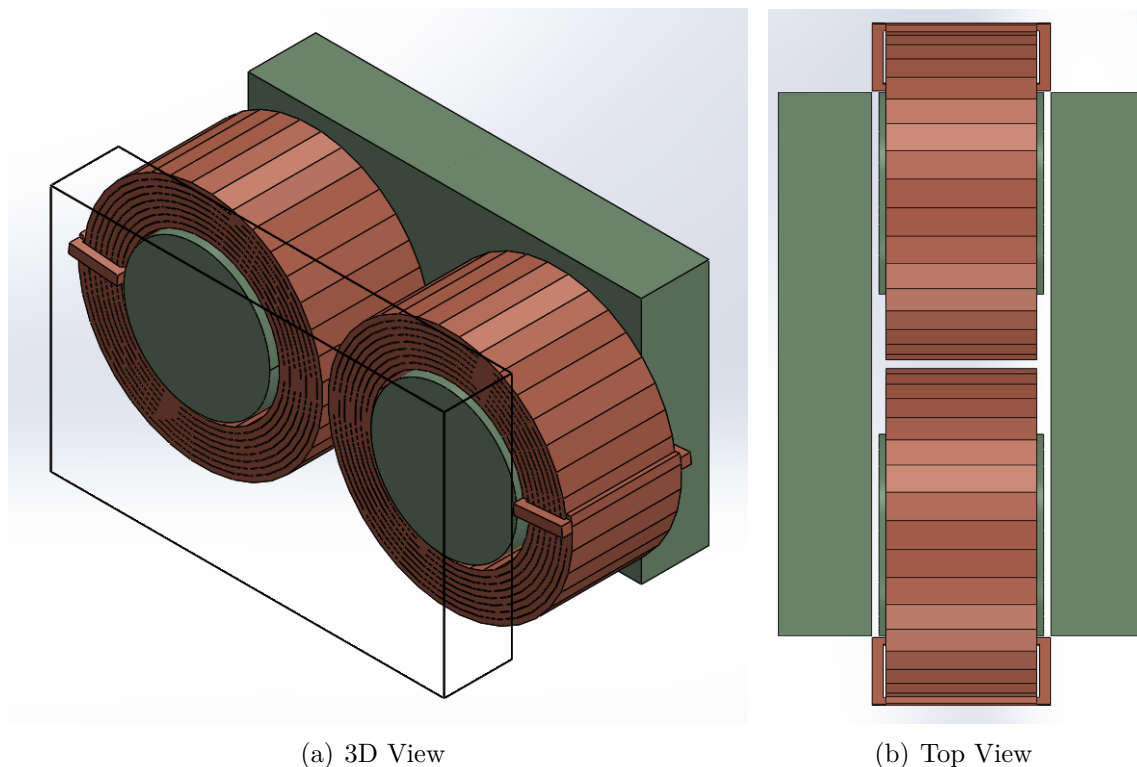


Figure 2.15: Final Coil Configuration

a model has to be developed which can be reliably built up in the LEA-lab. Critical components are the ferrite cores, because they have to be milled individually. Due to the provided information the milling machine in the LEA-lab is able to produce cubic and cylindrical components up to an accuracy of $1/100$ mm. Also the length of the air gaps has to be defined with high accuracy. For that purpose a fill material based on Aluminum-Nitrite shall be pressed or glued inbetween the air gaps.

Due to the implicit calculation of some geometry parameters during the process of simulation a couple of dimensions are not limited by a certain accuracy (except the precision of the used datatype in ANSYS). In Table 2.5 it can be seen that the dimensions of the leg width and the tablet radius are already rounded up to $1/100$ mm. As the ferrite components are critically in terms of saturation and it reduces some effort in producing it may be reasonable to round up to $1/10$ mm, so that it comes out with a tablet radius of 7.4 mm and a leg width of 6.9 mm.

2.8 Incorrections of the Simulation

Due to an error in calculating the resulting total inductance of the parallel connected two single coils to one inductor, the applied current ripples in the simulations summarized in Table 2.4 are not correct. Wrongly it has been assumed, that the self inductance values of both single inductors would have to be halved for a parallel connection of both coils. But this assumption only holds for a configuration with no mutual inductance, which equals two not coupled inductors. In terms of a transformer this means a coupling factor of $k = 0$ which equals a worst case scenario for the coupled inductor concerned in this project. The true inductance value must be higher than previously assumed. Therefore the current ripple must be smaller than assumed in the iteration of finding an optimal coil configuration. According to that the AC ohmic losses and the core losses are lower than determined before. All in all this leads to the conclusion that the figured out "optimal" design is definitely oversized.

2.8.1 Improved Simulation

To reevaluate the oversized final coil configuration, a modified simulation with physically coupled inductors is to be investigated in an FEM simulation. The CAD model is adjusted in the way Figure 2.16 shows. The two previously separate windings are now connected with the help of an additional copper block inbetween them. This allows to excite the simulation by a single current which ideally divides up into both parallel connected windings. This configuration does not need a post processing in terms of calculating the resulting total inductance value. The resulting inductance value of $8.0\ \mu\text{H}$ shows a coupling factor of 67% assuming a self inductance of $9.6\ \mu\text{H}$ considering two separate windings like in the previous simulation.

As expected, the corrected simulation leads to a higher total inductance value. According to that the lower AC ohmic and core losses lead to total losses of only 1.9 W compared to previously 2.7 W. Also the total maximal current ripple reduces from 51.4 A to 47.6 A. This leads to maximum mean magnetic flux density in the ferrite core of 288 mT compared to previously 309 mT.

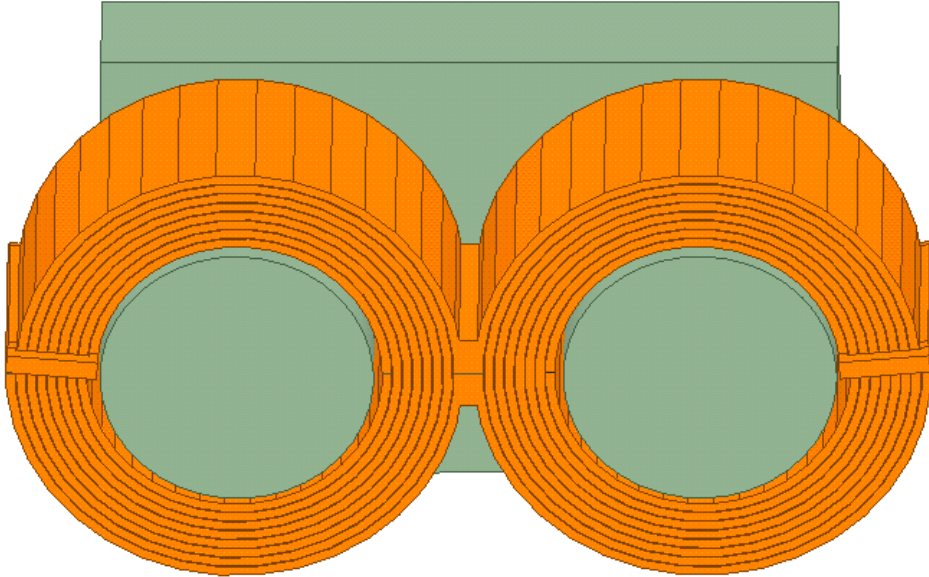


Figure 2.16: Improved CAD model of the coil

	L_{total}	ΔI	I_{peak}	B_{mean}	$P_{\Omega,\text{DC}}$	$P_{\Omega,\text{AC}}$	P_{core}	P_{total}
<i>old</i>	4.8 μH	18.8 A	51.4 A	309 mT	1.476 W	1.068 W	0.189 W	2.732 W
<i>new</i>	8.0 μH	11.5 A	47.6 A	288 mT	1.472 W	0.386 W	0.056 W	1.904 W

Table 2.6: Comparison of the corrected simulation with the previous optimal result

3 MOSFET Selection

Switches are an integral part of power electronic devices. For this project Si-MOSFETs are chosen as switching elements. Si-MOSFETs are mainly used in low and medium voltage range applications. Silicon technology has certain disadvantages in comparison to MOSFETs of SiC and GaN-technology but the easy availability of Si-MOSFETs in all low voltage ranges and lower price make it the choice of switch for this project. Moreover, Si-devices also show better efficiency while operating at low switching frequencies than their SiC and GaN counterparts.

On the other hand, another goal of the project is to produce a benchmark while comparing two converter realizations with GaN-MOSFETs and Si-MOSFETs respectively.

The choice of a specific MOSFET is made by investigating some important factors such as total losses, temperature and packaging.

3.1 Loss Descriptions and Approximations

In general, MOSFET losses comprise of switching loss, conduction loss, dead time loss and gate charge loss. For loss approximations, the drain-source on resistances of all shortlisted MOSFETs R_{DSon} are taken at gate-source voltage V_{gs} value of 10 V. Moreover, all the above mentioned losses are calculated at a duty cycle D of 25%, inductance of 4.80 (worst case approximation of inductance value as mentioned in Chapter 2) and switching frequency of 100 kHz.

Since the converter is bi-directional, it can operate both at continuous buck mode

as well as continuous boost mode. However, Continuous buck mode is the nominal operation for rated power of 2kW. Moreover, using continuous buck operating mode, the generation of highest losses in the MOSFETs are expected. On the other hand, at continuous boost mode, the rated operation may not be achieved. As a result, the losses are calculated considering the continuous buck mode operation.

The losses are calculated as stated in [8].

MOSFET Conduction Losses

Conduction losses occur in a MOSFET (or in any power switch) when the MOSFET operates in on-state. Conduction losses have a dependency on MOSFET drain-source on-resistances R_{DSon} and RMS value of drain current.

Moreover, R_{DSon} is also dependent on temperature as seen from Figure 3.4. As conduction losses are calculated as the function of R_{DSon} , it can also be inferred that conduction losses are temperature dependent as well.

During the converter application both high-side and low side MOSFET will exhibit conduction losses, the conduction loss approximations are done for both high-side and low-side MOSFETs.

For high-side MOSFET, conduction loss approximations are shown in Equation 3.1.

$$P_{con,H} = R_{DSon} I_{Drms,H}^2 \quad (3.1)$$

$I_{Drms,H}$ states the root mean square value of MOSFET drain current for high-side. $I_{Drms,H}$ can be further calculated as function of duty cycle D , ripple current Δi_L and output current I_{out} .

$$I_{Drms,H} = \sqrt{D(I_{out}^2 + \frac{1}{12}\Delta i_L^2)} \quad (3.2)$$

where, inductor current ripple Δi_L can be further calculated as a function of duty cycle

D , converter input voltage U_{DD} , switching frequency f_{sw} and inductance L .

$$\Delta i_L = \frac{D(1-D)U_{DD}}{f_{sw}L} \quad (3.3)$$

Subsequently, the conduction losses of low-side MOSFETs are stated in the Equation 3.4

$$P_{con,L} = R_{DSon}I_{Drms,L}^2 \quad (3.4)$$

$I_{Drms,L}$ states the root mean square value of MOSFET drain current for low-side. Moreover, the functional dependencies remain exactly same as the Equation 3.2.

$$I_{Drms,L} = \sqrt{(1-D)(I_{out}^2 + \frac{1}{12}\Delta i_L^2)} \quad (3.5)$$

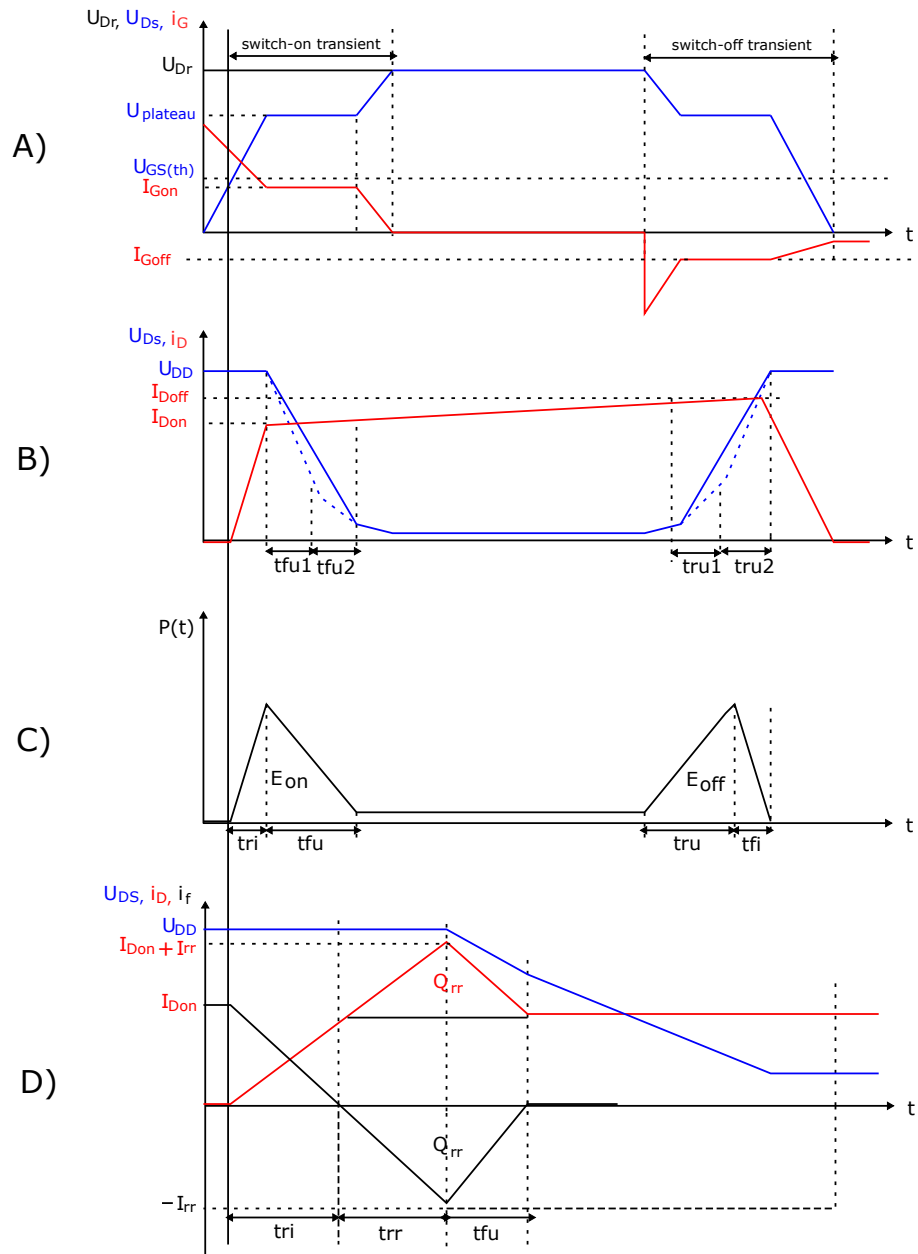
Switching Loss

Switching losses occur in MOSFETs (or in any power switches) when the MOSFET is transitioning from on-state to off-state and vice versa. The dependency of switching losses on several factors like switching voltage, switching current, switching frequency are further mentioned in the following Table 3.1. The timing diagrams of the switching losses can be illustrated in the following Figure 3.1

Switching losses are characterized by switching transients and the losses associated due to those transients along with the switching frequency. In the Figure 3.1 part A) states the switch-on and switch-off transients, B) states the drain-source voltage U_{DS} and drain current I_D without considering the reverse recovery of the free-wheeling into concern, C) states the qualitative overview of the turn-on and turn-off energies and D) shows the reverse recovery effects during the switching losses.

Approximations for switching losses are done considering several parameters, illustrated in Table 3.1

3 MOSFET Selection



Parameter Symbol	Meaning
U_{DD}	Converter Input Voltage
U_{DS}	Drain Source Voltage
U_{Dr}	Driver Output Voltage
t_{ri}	Current Rise Time
t_{fi}	Current Fall Time
t_{ru}	Voltage Rise Time
t_{fu}	Voltage Fall Time
Q_{rr}	Reverse Recovery Charge
f_{sw}	Switching Frequency

Table 3.1: Description of the variables used for switching loss calculation

Switching losses in MOSFETs are calculated taken turn-on energy, turn off energy of the MOSFET and switching frequency into consideration. Moreover, switching losses are calculated for high-side MOSFETs. Since the converter is targeted to operate at continuous buck mode for rated power of 2kW, in this operating strategy the low-side MOSFETs are switched on at zero voltage. Hence the switching losses at the low-side MOSFETs can be neglected.

The approximation for turn-on energy in MOSFET is illustrated in the Equation 3.6.

Turn-on Energy Losses in MOSFET

$$E_{on,M} = \int_0^{t_{ri}+t_{fu}} u_{DS}(t)i_D(t)dt = U_{DD}I_{D,on}\frac{(t_{ri} + t_{fu})}{2} + Q_{rr}U_{DD} \quad (3.6)$$

$E_{on,M}$ signifies the turn-on energy of the MOSFET. Furthermore, voltage fall time t_{fu} is calculated as the median of two voltage fall times t_{fu1} and t_{fu2} defined through the gate current $I_{G,on}$ and gate capacitances namely C_{GD1} and C_{GD2} . The procedure to determine the above stated gate capacitances is shown in Figure 3.2. The drain-source voltage during the fall time and the place where the two-point approximation being taken into account, is shown in Figure 3.1B with the dotted line. Since this approximation is used only to determine the voltage fall time (as well as the rise time during switch off) and the drain-source voltage is assumed to have the linear form (solid line in Figure 3.1), it becomes clear that this analysis presents the worst case for the switching

losses calculation [8].

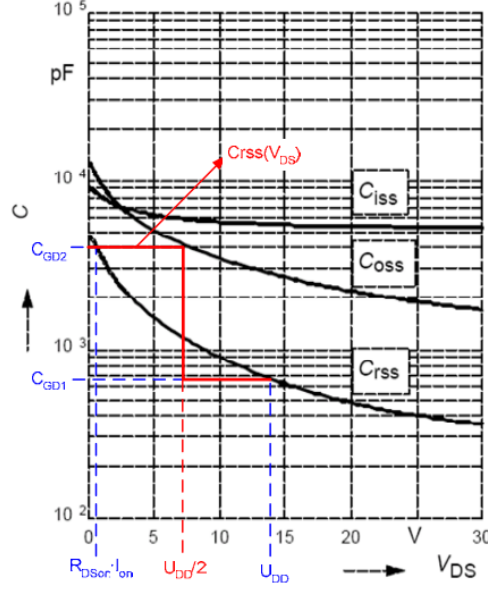


Figure 3.2: Two point approximation of gate-drain capacitance to calculate voltage rise time and voltage fall time [8]

The gate current during voltage fall time can be calculated with driver output voltage U_{Dr} , Miller plateau voltage $U_{plat.}$ and gate resistance R_G . The value of gate resistance is taken as suggested in the respective datasheets of the shortlisted MOSFETs.

$$I_{G,on} = \frac{U_{Dr} - U_{plat.}}{R_G} \quad (3.7)$$

The respective voltage fall times t_{fu1} and t_{fu2} at two different gate capacitances can be further illustrated by the following equations.

$$t_{fu1} = (U_{DD} - R_{DSon}I_D) \frac{C_{GD1}}{I_{G,on}} \quad (3.8)$$

$$t_{fu2} = (U_{DD} - R_{DSon}I_D) \frac{C_{GD2}}{I_{G,on}} \quad (3.9)$$

As a result, the voltage fall time can be obtained as.

$$t_{fu} = \frac{t_{fu1} + t_{fu2}}{2} \quad (3.10)$$

Turn-off Energy Losses of MOSFET

$$E_{\text{off,M}} = \int_0^{t_{\text{ru}}+t_{\text{fi}}} u_{\text{DS}}(t) i_{\text{D}}(t) dt = U_{\text{DD}} I_{\text{Doff}} \frac{(t_{\text{ru}} + t_{\text{fi}})}{2} \quad (3.11)$$

$E_{\text{off,M}}$ signifies the turn-off energy of the MOSFET. The calculation procedure of voltage rise time t_{ru} and the approximations of gate capacitances are exactly the same as mentioned for voltage fall time t_{fi} .

The gate turn of current can be calculated as

$$I_{\text{G,off}} = -\frac{U_{\text{plat.}}}{R_{\text{G}}} \quad (3.12)$$

The above mentioned voltage rise times through the gate capacitances C_{GD1} and C_{GD2} calculated as.

$$t_{\text{ru1}} = (U_{\text{DD}} - R_{\text{DSon}} I_{\text{D}}) \frac{C_{\text{GD1}}}{I_{\text{G,off}}} \quad (3.13)$$

$$t_{\text{ru2}} = (U_{\text{DD}} - R_{\text{DSon}} I_{\text{D}}) \frac{C_{\text{GD2}}}{I_{\text{G,off}}} \quad (3.14)$$

With these parameters, the voltage rise time t_{ru} is calculated as.

$$t_{\text{ru}} = \frac{t_{\text{ru1}} + t_{\text{ru2}}}{2} \quad (3.15)$$

MOSFET Switching Losses

With all the sub-formulas together, the total switching losses of a MOSFET (for high-side in this converter application) P_{sw} can be stated as follows.

$$P_{\text{sw}} = (E_{\text{on,M}} + E_{\text{off,M}}) f_{\text{sw}} \quad (3.16)$$

Deadtime Loss (Body Diode Conduction Losses)

To prevent a short circuit, a deadtime is set to turn-off both high-side and low side MOSFET, although the inductor current flows continuously. Deadtime losses (body diode conduction losses) occur at the switching intervals where the interlocking for the deadtime is. Deadtime losses can occur both at the body diodes high-side and low-side MOSFETs depending upon the operating point. During deadtime the inductor current flows through the either of the body diodes (high-side or low side), inturn generates the body-diode conduction losses[9]. The Figure 3.3 refers to the operating modes of a bi-

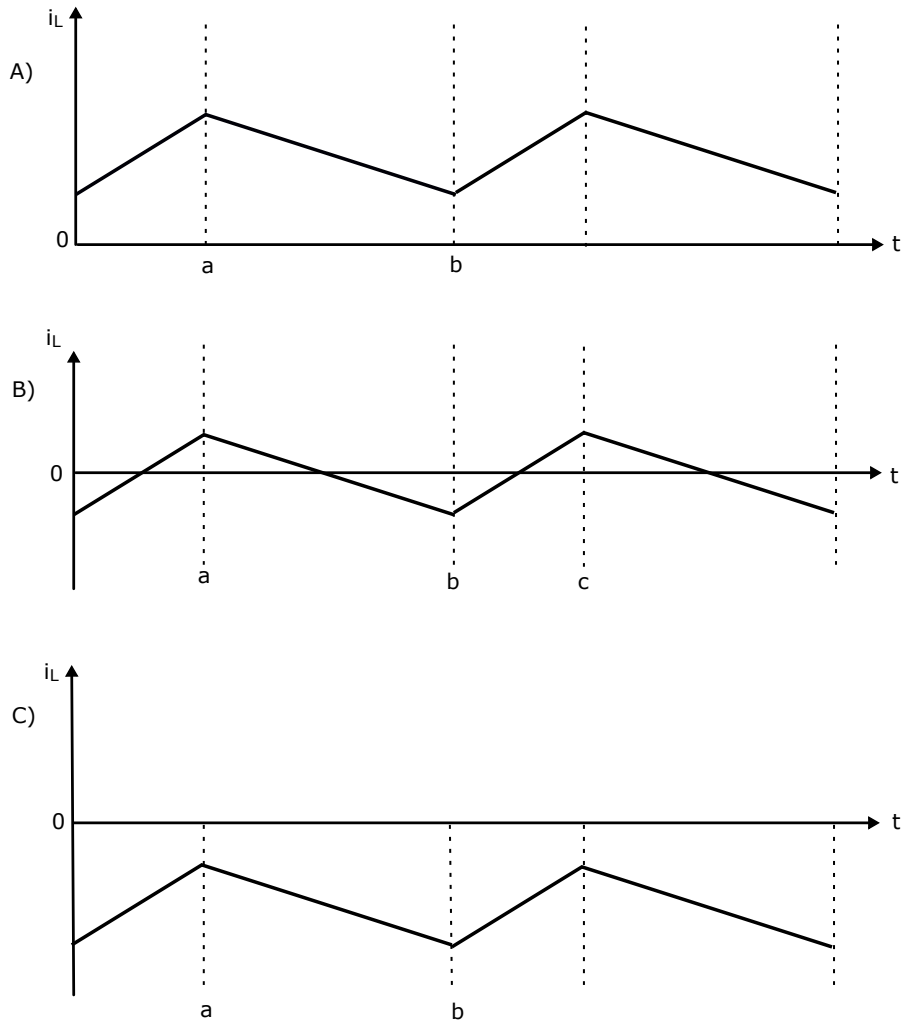


Figure 3.3: Operating strategy of bi-directional DC-DC converter

directional converter. Here, mode-A) signifies continuous buck mode , mode-B) signifies the discontinuous conduction mode and mode-c) signifies the continuous boost mode.

When the converter is operating at mode-A), where the current is fully positive, the body diode conduction losses occur at the body diodes of the low side MOSFETs (a very short interval at point a and very short interval at point b as per Figure 3.3 at mode-A) i.e. at low power mode the deadtime losses occur at both body diodes of high-side and low-side MOSFETs. At low power mode, when the interlocking points are below the zero line then the upper body diode shows deadtime losses and when it is above zero the lower body diode shows the deadtime losses. (at mode-C), where the current is fully negative, the deadtime losses occur at the body diodes of the high-side MOSFETs.

As mentioned earlier, continuous buck mode is the nominal operation for the converter and rated operation of 2 kW is targeted with this operating point, hence the deadtime losses are calculated for the low side MOSFETs only. The formula to calculate deadtime losses P_D are stated as.

$$P_D = V_D I_O (t_{dr} + t_{df}) f_{sw} \quad (3.17)$$

V_D signifies the forward voltage of low-side MOSFET body diode, I_O signifies the output current, t_{dr} and t_{df} are deadtime at rising and dead time at falling respectively and f_{sw} is the switching frequency.

As an example, the MOSFET BSC-01 (nomenclature and other informations are elaborated in Table 3.2) exhibit deadtime losses (body diode conduction losses losses) of approximately 0.19 W.

MOSFET Gate Charge Losses

Gate charge loss P_g comprises of the loss associated with MOSFET gate charging [9]. Gate charge loss is dependent of the gate electric charge or the gate capacity of high-side and low-side MOSFETs, gate voltage V_{gs} , and switching frequency f_{sw} . Gate charge loss can be calculated using the following equation.

$$P_g = (Q_{g,H} + Q_{g,L}) V_{gs} f_{sw} \quad (3.18)$$

$Q_{g,H}$ and $Q_{g,L}$ are gate charges of high-side and low-side MOSFETs respectively.

$$P_g = (C_{g,H} + C_{g,L})V_{gs}^2 f_{sw} \quad (3.19)$$

$C_{g,H}$ and $C_{g,L}$ are gate capacitance of high-side and low-side MOSFETs respectively.

For example, the MOSFET BSC-01 (nomenclature and other informations are elaborated in Table 3.2) exhibit gate charge losses of approximately 0.0215 W.

Body Diode Switching Losses

since, the switch-off energy $E_{off,D}$ in diode is normally neglected ($E_{off,D} = 0$) [8], so the body diode switching losses can be calculated only taking diode turn on energy $E_{on,D}$ and switching frequency f_{sw} into account. The approximations for diode turn on energy can be stated in the Equation 3.21.

$$E_{on,D} = \int_0^{t_{ri}+t_{fu}} u_D(t)i_F(t)dt = E_{onDrr} = \frac{1}{4}Q_{rr}U_{Drr} \quad (3.20)$$

U_{Drr} states about the voltage across the diode during the reverse recovery. For worst case calculations this above mentioned voltage can be approximated with the supply voltage ($U_{Drr} = U_{DD}$) [8].

The total diode switching losses P_{total} is stated as.

$$P_{sw,D} = (E_{on,D} + E_{off,D}) * f_{sw} = E_{on,D} * f_{sw} \quad (3.21)$$

For example, the calculated diode switching losses of MOSFET BSC-01 (nomenclature and other informations are elaborated in Table 3.2) is approximately 0.103 W.

Since, the gate charge losses and deadtime losses are lower than both switching and conduction losses, to further proceed with the loss calculations, the focus is put on switching losses and conduction losses.

The above mentioned losses are calculated for one high-side MOSFET and subsequently for one low-side MOSFET.

MOSFET Losses at High-Side

For the high-side MOSFETs both turn on and turn off losses are prominent. MOSFET losses at high-side $P_{\text{total,H}}$ is calculated as the summation of high-side MOSFET conduction losses $P_{\text{con,H}}$ and subsequent switching losses P_{sw} .

$$P_{\text{total,H}} = P_{\text{con,H}} + P_{\text{sw}} \quad (3.22)$$

MOSFET Losses at Low-Side

The low side MOSFET will only exhibit turn off losses. As mentioned earlier, for continuous buck mode operation (mode-A as per Figure 3.3) at rated power the low side MOSFET will be switched on at zero voltage. As a result the turn-on losses in low side MOSFETs can be neglected. Hence, the losses at the low side MOSFET $P_{\text{total,L}}$ will be equal to the conduction losses at low-side MOSFET $P_{\text{con,L}}$.

$$P_{\text{total,L}} = P_{\text{con,L}} \quad (3.23)$$

Total Diode Losses

Total diode losses P_{Dt} can be stated as the following.

$$P_{\text{Dt}} = P_{\text{D}} + P_{\text{sw,D}} = P_{\text{D}} + E_{\text{on,D}}f_{\text{sw}} \quad (3.24)$$

P_{D} and $E_{\text{on,D}}$ are body diode conduction losses and turn on energy of the body diode respectively. Switch-off energy losses in diode are normally neglected [8].

The calculated body diode losses of the above stated MOSFET BSC-01 comes in the vicinity of approximately 0.3 W.

Losses Per Rail Due to Switches

Subsequently, conduction losses at both high-side ($P_{\text{con,H}}$) and low-side MOSFETs ($P_{\text{con,L}}$) along with the switching losses at high-side MOSFET (P_{sw}) contribute for the total losses per rail (P_{rail}).

$$P_{\text{rail}} = P_{\text{con,H}} + P_{\text{sw}} + P_{\text{con,L}} = P_{\text{total,H}} + P_{\text{total,L}} \quad (3.25)$$

where, $P_{\text{total,H}}$ and $P_{\text{total,L}}$ are total losses occurrence at high-side and low-side MOSFETs respectively.

Furthermore, the total body diode losses are neglected since they are much lower compared to total MOSFET losses.

The loss calculation workflow is stated in the following Figure 3.4.

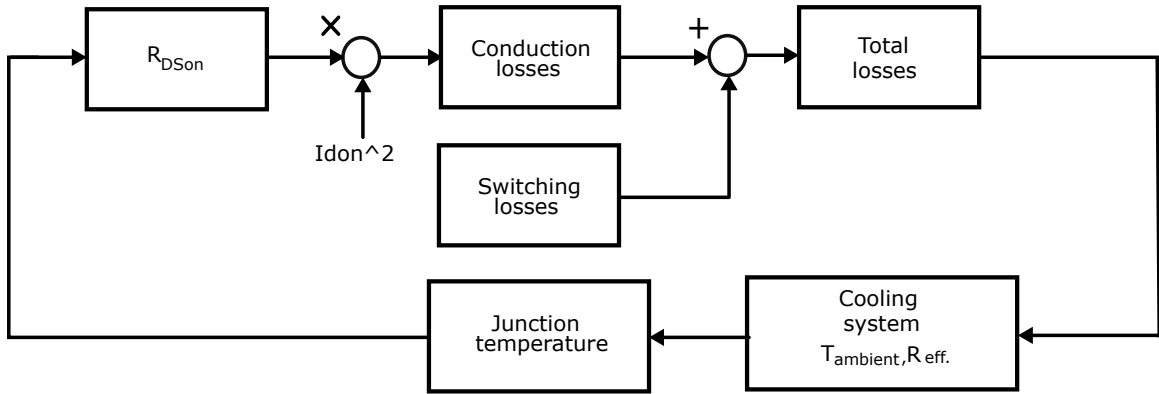


Figure 3.4: Loss calculation workflow

As the flowchart suggests, from the total losses, the junction temperatures T_{new} of the shortlisted MOSFETs are calculated iteratively as the MOSFET drain-source on resistances $R_{\text{ds,on}}$ are dependent on temperature. The ambient temperature T_{ambient} is chosen as 60°C for heat sink. Typically 60°C temperature value is assumed for water-cooling in automotive applications.

The thermal resistances $R_{\text{th,new}}$ of the Si-MOSFETs are calculated based on the assumption that thermal resistances of vias, TIM material and housing, which in total constructs the effective thermal resistance R_{eff} , will behave similar to that in [2]. The

thermal equivalent circuit duly illustrates the parameters based on which the thermal approximations are done [2]. This can be well visualized from the Figure 3.5.

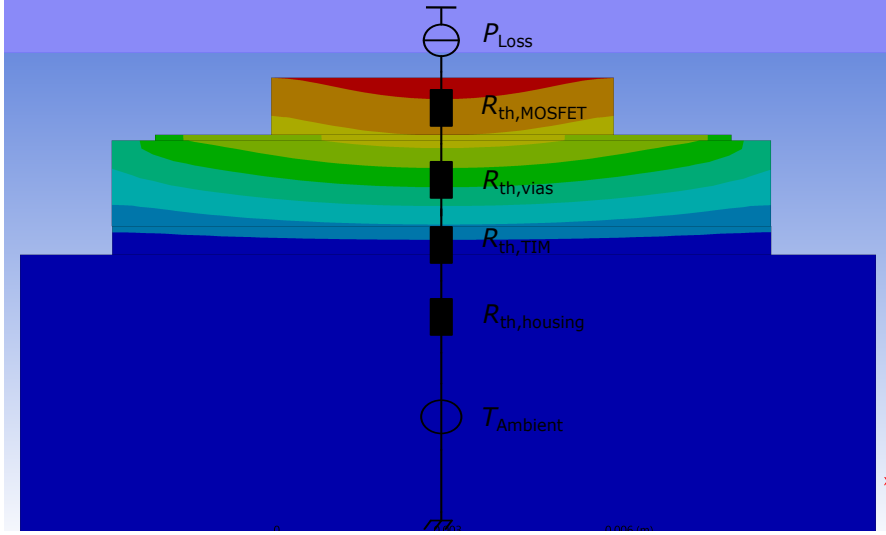


Figure 3.5: Two dimensional cut of thermal equivalent circuit of the MOSFET along with the thermal resistance of vias, TIM material and housing.

Besides the above mentioned parameters, the junction to case thermal resistance of the listed MOSFETs R_{jc} , area of GaN MOSFET-pads used for cooling A_{GaN} along with the cooling area of Si MOSFETs-pads A_{new} are also taken into account while calculating the thermal resistance of the Si-MOSFETs.

$$R_{th,new} = R_{eff} \frac{A_{GaN}}{A_{new}} + R_{jc} \quad (3.26)$$

From the calculated thermal resistance as per Equation 3.26 and the losses, the junction temperatures of each MOSFET are calculated as. Furthermore, the junction temperatures are calculated taking the highest losses into consideration. To be more precise, cases where high-side MOSFET losses are more than that of low-side, the junction temperatures can be approximated as.

$$T_{new} = T_{ambient} + P_{total,H} R_{th,new} \quad (3.27)$$

Similarly, cases where the low-side MOSFET losses are higher than the high-side ones, the junction temperatures can be approximated as.

$$T_{\text{new}} = T_{\text{ambient}} + P_{\text{total,L}} R_{\text{th,new}} \quad (3.28)$$

3.2 Comparative Loss Calculation and Temperature Calculation Analysis

After iteratively calculating the losses per rail, the highest temperatures of either of the MOSFETs and comparing the values, the best MOSFET is chosen for our applications.

To compare the MOSFETs by the means of junction temperature values, a maximum safety margin of 25 °C has been assumed. As an example, if the maximum operating junction temperature of a MOSFET as per data sheet ($T_{\text{j,max}}$) is 150 °C, then the ideal operating junction temperature ($T_{\text{j,ideal}}$) from the losses should be around, $T_{\text{j,ideal}} = T_{\text{j,max}} - T_{\text{safety}}$ i.e. 125 °C to ensure its safe operation.

The comparison of total losses per rail and calculated temperatures of either high-side or low-side MOSFETs, depending upon which one shows highest losses, are illustrated in the Figure 3.6. Moreover, the abbreviations used to denote the MOSFETs are further illustrated in the Table 3.2.

From the graphs it can be observed that, inspite of having total loss values within approximately 10 W, the MOSFETs BSC-03, CSD-01, BSC-04, BSC-05 and BSC-06 show a very high temperature value around 150 °C. Keeping the safety margin in mind, it can be noted that the calculated temperatures surpass the maximum ideal operating temperature. If there is a rise in temperature due to mechanical or electrical activities, these MOSFETs cannot cope up with the rising temperature and may get destroyed. Hence these MOSFETs can be discarded.

A contradiction can be spotted while looking at IPT-02 and IPT-04. Both the IPT-

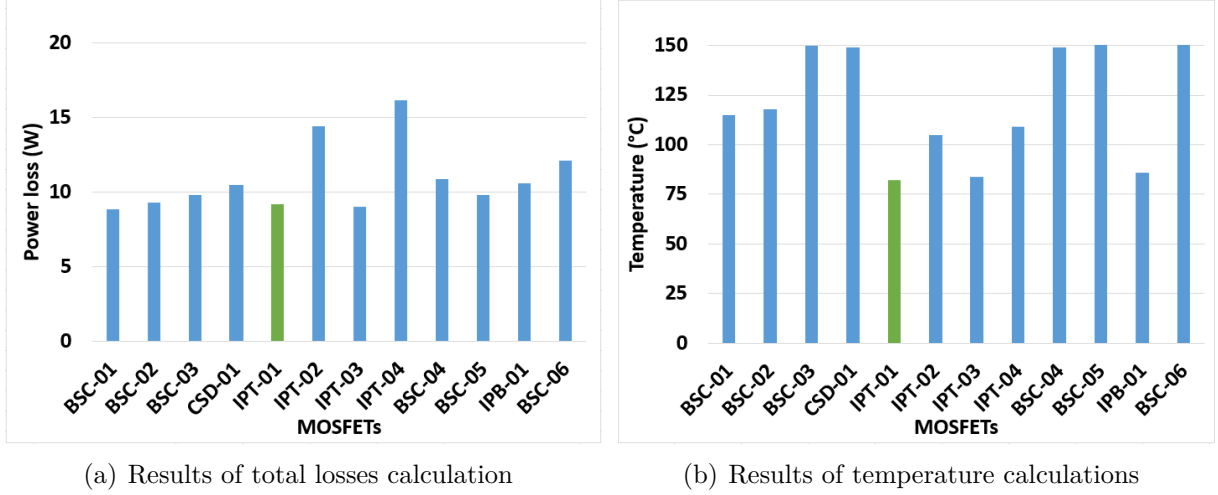


Figure 3.6: Graphical comparison of total losses and temperatures calculated at 100 kHz switching frequency. The green bar indicates the chosen MOSFET for the converter application.

Abbreviation	MOSFET	Package	Manufacturer
BSC-01	BSC040N08NS5	TD-SON	Infineon Technologies
BSC-02	BSC037N08NS5	TD-SON	Infineon Technologies
BSC-03	BSC021N08NS5	TD-SON	Infineon Technologies
CSD-01	CSD19502Q5B	TD-SON	Texas Instruments
IPT-01	IPT026N10N5	HSOF	Infineon Technologies
IPT-02	IPT015N10N5	HSOF	Infineon Technologies
IPT-03	IPT020N10N5	HSOF	Infineon Technologies
IPT-04	IPT020N10N3	HSOF	Infineon Technologies
BSC-04	BSC027N10NS5	TD-SON	Infineon Technologies
BSC-05	BSC025N08LS5	TD-SON	Infineon Technologies
IPB-01	IPB024N10N5	HSOF	Infineon Technologies
BSC-06	BSC035N10NS5	TD-SON	Infineon Technologies

Table 3.2: Illustration of Abbreviations used to specify the MOSFETs. The green marked row indicates the chosen MOSFET for the converter application.

series MOSFETs show the approximate temperature value of 105 °C which is within the maximum ideal operating temperature limit. But while looking at the figure 3.6(a) it can be seen that, both the MOSFETs show a total loss of almost 15 W per rail. With four rails operating synchronously, the total converter losses due to switches will be around 60 W. Such high losses will result in poor converter efficiency, which makes IPT-02 and IPT-04 inapt for the converter application.

The loss occurrences in the remaining MOSFETs are almost similar to each other (as per 3.6(a)). Hence a clear conclusion cannot be drawn while selecting the best MOSFET for the converter application only based on total losses. While from the figure 3.6(b) it can be seen that, the calculated temperature values are within the ideal operating temperature limit as well. Hence for further comparison, packaging size and cost of each MOSFET are taken into account. The comparison is further illustrated in the Table 3.3.

MOSFET	Loss (W)	Temperature (°C)	Package size (mm ²)	Price (€)*
BSC-01	8.92	115	14	1.62
BSC-02	9.34	118	14	1.98
IPT-01	9.23	82	50	3.63
IPT-03	9.06	85	50	4.77
IPB-01	10.6	88	50	3.98

**Price has been taken from <https://www.mouser.de/> and for a single piece dated on 21-06-2020*

Table 3.3: Comparison of further shortlisted MOSFETs of having similar parameters. The green marked row indicates the chosen MOSFET for the converter application.

As per Table 3.3, it can be seen that BSC-series MOSFETs possess smaller pad size, hence using the BSC-series MOSFETs will result in the overall reduction in PCB size. Furthermore, the prices per piece of both BSC-series MOSFETs are almost half as high as the IPT-series. As one of the goals of the project is to realize the converter in a cost efficient way, considering all of these parameters BSC-series MOSFETs can be chosen for converter application.

A deeper observation also states that between the two BSC-series MOSFETs, BSC-

01 show better values in terms of all mentioned parameters shown in the Table 3.3 than BSC-02. Moreover BSC-01 stands out when it is compared to IPT-01 and IPT-03 in terms of loss, packaging size and price. Keeping all these factors in mind it is concluded that BSC-01 is the overall better choice than other MOSFETs for the converter application.

However, when the switch selections were done initially, the calculations were done for a switching frequency of 200 kHz. The graphical results are given as following

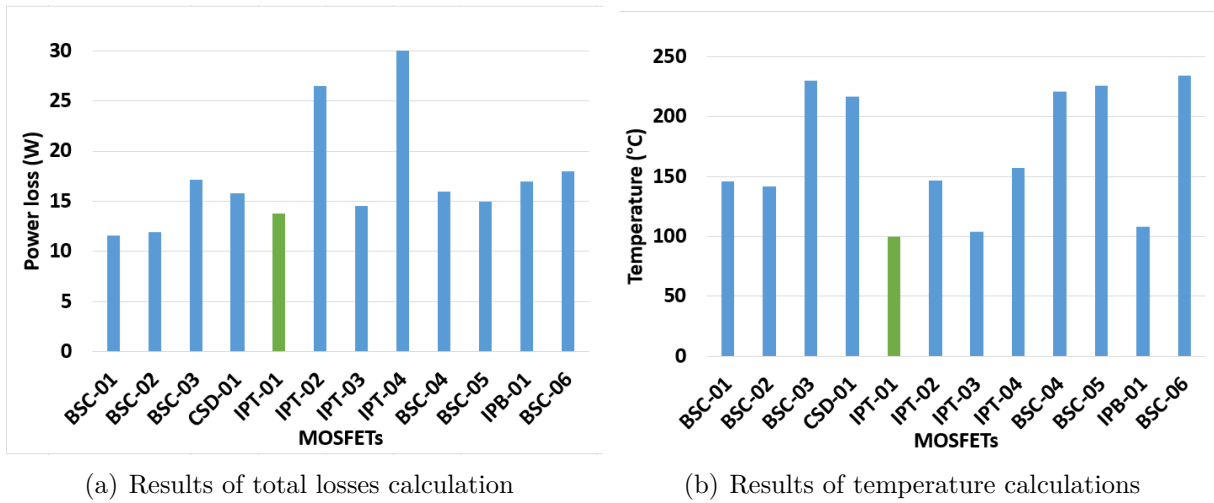


Figure 3.7: Graphical comparison of total losses and temperatures calculated at 200 kHz switching frequency. The green bar indicates the chosen MOSFET for converter application.

As per the 3.7(b) the BSC-01 and BSC-02 showed worse temperature parameters in comparison to the IPT-01, IPT-03 and IPB-01. In each case the two above mentioned BSC-MOSFETs exceeded the ideal operating temperature limit. As a result they were discarded.

Further comparing the remaining IPT-MOSFETs, IPT-01 showed better parameters in terms of temperature and cost. As a result, IPT-01 had been chosen for the converter application. As the PCB layout and inductor design are done keeping the IPT-01 in mind, as a result it is decided by the project group to go ahead with the previous chosen MOSFET.

4 Schematic and Layout

4.1 Schematic

Due to silicon semiconductor device selected for this semester, rather than the previously used GaN semiconductor, a new schematic is needed. Also as mentioned earlier, the power rating of the new converter is 2 kW, which requires increased copper area. The design of the new magnetic component with coupled magnetic concept, needs to be integrated with the PCB. This is briefly discussed in the section below.

4.1.1 Component Selection

To reduce the PCB size in spite of larger silicon semiconductor devices used, smaller components are needed. The given Table 4.1 summarizes the major component changes compared to previous semester project, along with its few important parameters like current ratings and power dissipation.

Gate Driver Circuit

The sizing of fundamental components of the gate driver circuit, such as the bootstrap circuit is discussed in this section. Reliable operation of the half-bridge is achieved by overcoming the effects presented by parasitic elements of the half-bridge. A bootstrap circuit is the proposed solution for a reliable operation. The bootstrap supply is formed by a capacitor and a diode. Proper dimension of the bootstrap capacitor, denoted as

Component	Component Type	Important Parameter
IRS2011	Gate Driver	Gate Current 19.2 mA
LM2575HVS	Switching Regulator 12 V to 48 V	Min Current Rating 77 mA
WSK1216L5000FEA	Shunt Resistor 0.5 m Ω (4 Terminal)	Power Dissipation 0.882 W

Table 4.1: Component list including its current rating and power dissipation

(C_{BOOT}), is necessary for flexible on-time and duty cycle. To size this capacitor, the minimum voltage drop, denoted as ΔV_{BS} , and the total charge required to charge the parasitic input capacitance of the MOSFET, denoted as Q_{TOT} , needs to be established. For the MOSFET chosen the $Q_{TOT} = 172$ nC and the minimum voltage drop $\Delta V_{BS} = 2.075$ V. The gate resistor value was taken directly from the transistor data-sheet. This gate resistor would be tuned experimentally according to the on-time (T_{ON}) and off-time T_{OFF} requirements. The calculations of important components are summarized in the Table 4.2.

Component	Value	Rating
Bootstrap Capacitor ($C_{BOOT(min)}$)	$C_{BOOT(min)} = \frac{Q_{TOT}}{\Delta V_{BS}}$	100 nF
Bypass Capacitor	10 C_{BOOT}	1 μ F
Gate Resistor	$T_{ON}=17$ ns	1.8 Ω

Table 4.2: Gate driver component ratings

Power Supply Circuit

To supply the gate driver voltage and other auxiliary voltage levels, linear voltage regulators as well as switching regulators were selected ,with the required current ratings, to derive different voltage level from the converter input/output. Since the converter is bidirectional, the power supply of the gate driver and micro-controller should be capable of starting the converter from the high voltage as well as low voltage side of the converter. 10 V to 15 V is sufficient to drive the transistor for converter operation. A

discharged Pb-accumulator has a voltage of about 10.8 V, which would be enough to drive the converter, although at a higher conduction losses. During the layout of the power supply circuits, the trace widths were chosen such that the voltage drop would be minimum, in order to ensure that the driver is operated as expected. The sizing of the auxiliary components of the switching regulator was necessary for its reliable operation. The reverse voltage of the diode, denoted as V_R , and the maximum input voltage of our application, denoted as $V_{i/p(MAX)}$, are important parameters to size the diode. A Schottky-diode is chosen since it has a low forward voltage and hence a lower loss. The component summary given in Table 4.3.

Component	Criteria	Value
Capacitor	Voltage Rating 18 V to 25 V	1 μ F
Schottky-Diode	$V_R = 1.25 * V_{i/p(MAX)}$	$V_R = 60$ V
Inductor	Voltage Rating=48 V Current Rating=0.4 A	1.5 mH

Table 4.3: Switching regulator component ratings

4.2 Layer Stack-up

The new DC-DC converter with a power rating of 2 kW has the full load current rating of 42 A on the 48 V side and 167 A on the 12 V side of the converter. Previously designed converter rated at 1 kW used a 4 layer stack-up. Due to higher converter rating, layer stack-up with higher current carrying capacity is required. In order to limit the temperature rise to 30 °C with an ambient temperature of 60 °C, increase in the number of layer is required. According to calculations, 142 mm and 21 mm trace width is required to carry 167 A and 42 A of currents respectively, in the inner layers with 105 μ m copper thickness. The calculation for the layer thicknesses and trace widths are summarized in the Table 4.4.

A power layer can be defined in order to achieve the desired temperature limit according to standard. Two possible layer stack-ups would be possible to limit the temperature rise in the PCB, 6-layers as given in Table 4.6 and 8-layers as given in Table 4.7.

Current Rating	Copper Thickness Internal Layer	Trace Width Internal Layer	Copper Thickness External Layer	Trace Width External Layer
167 A	105 μm	142 mm	35 μm	167 mm
42 A	105 μm	21.1 mm	35 μm	24.3 mm

Table 4.4: Trace width calculated using trace width calculator [10]

Constrains	Value
Ambient Temperature	60 $^{\circ}\text{C}$
Temperature Rise	30 $^{\circ}\text{C}$

Table 4.5: Temperature constrain used for the calculation of the trace width for current ratings in Table 4.4

4.3 Basic Layout

A basic layout Figure 4.1 was created on inkscape in order to map the component placement and to estimate the dimensions of the printed circuit board. The trace widths were calculated according to IPC-2221 standards[10]. The printed circuit board must be designed such that it would be capable of conducting 42 A current per rail and 167 A of full load output current, with the temperature rise limited up to 30 $^{\circ}\text{C}$ in an ambient temperature of 60 $^{\circ}\text{C}$. Since the layout process was started while drawing the basic layout, the sizes of components were decided according to the footprint on the layout. Approximate arrangement of the circuit was applied on Altium layout to get the dimensions of auxiliary circuits. The final PCB dimension is 151 mm \times 101 mm.

Semiconductor Devices

The MOSFET placement shown in Figure 4.2 serves two purposes. It helps to reduce the commutation and gate-driver area and also saves space on the PCB. As shown, vias are placed underneath the transistors for good current conduction into the inner layers as well as for thermal relief. This compact arrangement is used for all the four rails of the interleaved DC-DC converter.

Layer	Layer Name	Thickness
	Top Solder	
Layer 1	Top Layer	35 μ m
	Dielectric	
Layer 2	GND Layer	105 μ m
	Dielectric	
Layer 3	Power Layer	105 μ m
	Dielectric	
Layer 4	Power Layer	105 μ m
	Dielectric	
Layer 5	GND Layer	105 μ m
	Dielectric	
Layer 6	Bottom Layer	35 μ m
	Bottom Solder	
Minimum thickness		1.55mm
Price		559 € [11]

Table 4.6: 6-Layer Stack-up [12]

Layer	Layer Name	Thickness
	Top Solder	
Layer 1	Top Layer	35 μ m
	Dielectric	
Layer 2	GND Layer	105 μ m
	Dielectric	
Layer 3	Power Layer	105 μ m
	Dielectric	
Layer 4	Power Layer	105 μ m
	Dielectric	
Layer 5	Power Layer	105 μ m
	Dielectric	
Layer 6	Power Layer	105 μ m
	Dielectric	
Layer 7	GND Layer	105 μ m
	Dielectric	
Layer 8	Bottom Layer	35 μ m
	Bottom Solder	
Minimum Thickness		2.4mm
Price		646 € [11]

Table 4.7: 8-Layer Stack-up [12]

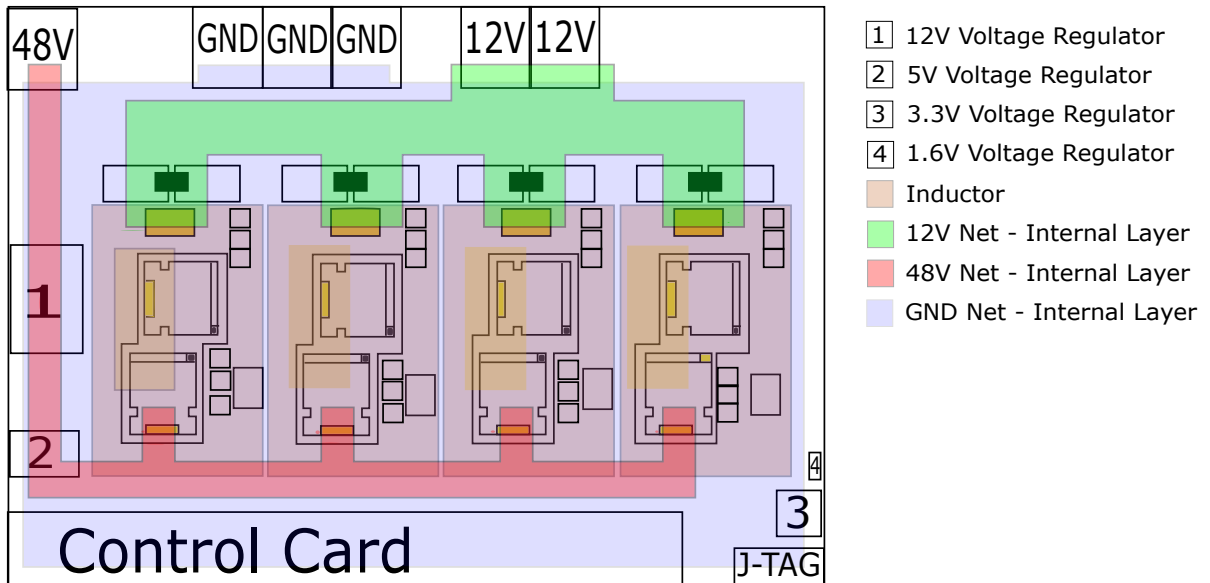


Figure 4.1: Basic Layout Overview

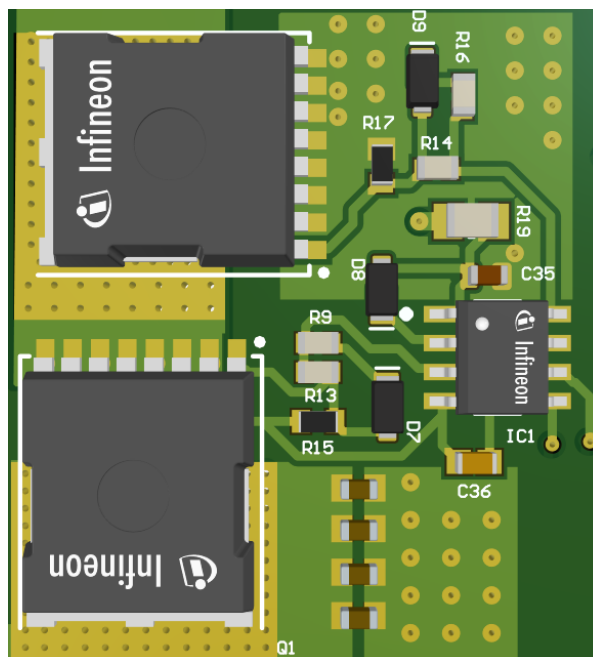


Figure 4.2: Placement of MOSFETs

Gate Driver and Current Measurement Circuit

Aim was to reduce the commutation loop, so the input capacitors were placed as close as possible to the switches on the bottom surface as well as on the top surface. The gate driver was placed close to the switches in an alignment with smaller area of the gate-source loop. The output capacitors must be placed closer to the inductor. While connecting the traces on the layout the current flow must be optimized, such that the current flow path is short and direct. The current measurement circuit was placed on the bottom layer in order to reduce the electromagnetic interference due to the inductor, which is placed on the top side just over the semiconductor and driver circuit arrangement.

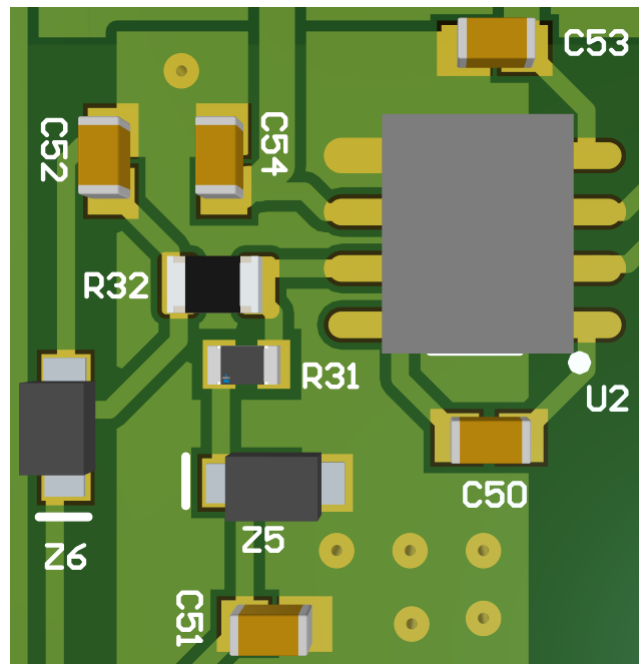


Figure 4.3: Layout of Current Measurement Circuit on the PCB

Inductor Placement

Placement of the new inductor topology, used for the project, is an important topic of discussion, due to its different winding topology. There are 4 terminals of an

inductor assembly for one rail. There are two possibilities to connect these terminals. One approach is to place 4 copper pads on the PCB for each inductor terminal and connecting the two input and the two output terminals on the PCB through traces or polygon pour. The other approach is to connect the two input and the two output terminals externally or internally through jumpers and copper sheets and include only one inductor pad for input and output each on the PCB. Due to the space constrain, the later approach is chosen. The inductor, placed just above the switches is given in Figure 4.4. The inductor pads are 2.4mm apart. Dimensions of pads are 8.9 mm x 4.8 mm.

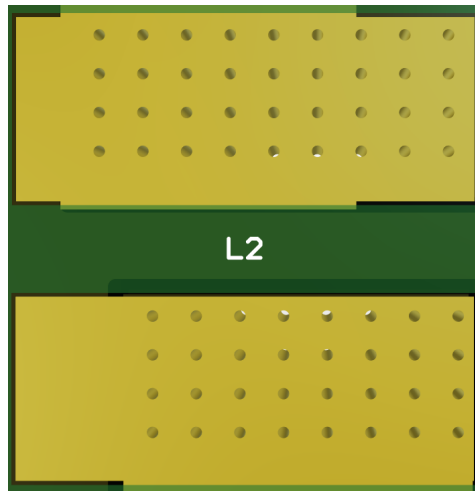


Figure 4.4: Inductor Pads

5 Control Hardware Selection

The choice of control hardware is very important regarding capabilities in terms of signal measurement, processing and controlling the power electronic hardware but also regarding the size and integration of the control hardware itself. While earlier project groups like summer term 19 [13] and winter term 18/19 [5] used a F28379D-Launchpad, which is very computationally powerful and offers many utility features, winter term 19/20 [2] chose a F28335-Card. This is done to take advantage of its smaller volume and the option to place it upright on the PCB, which can be seen in Figure 5.1.

However, while the manufacturer still supplies the F28335-Card and other control cards with a DIMM100 connector, the connector itself is not available anymore, making it a bad choice for future projects. According to consultations with Texas Instruments they recommend to use one of the newer generation control cards which have a 180-pin HSEC connector. Table 5.1 shows a comparison of important features for the previously used F28335-Card and these newer cards. The F280025C-Card is not considered in this comparison because at the time of this report it is a prototype and has limited availability. However, in the future it could be considered as a cheap alternative.

All of the newer control cards in Table 5.1 show similar or better parameters than the old F28335-Card which means that all of them have the necessary computing power and peripherals to be used for the converter. Furthermore, all of these cards offer an XBAR-architecture and Trip-Zone detection with post-processing blocks that have integrated comparators. These are important utility features, which are explained in [2, p. 26], and allow for the overcurrent-protection circuit added in that project to be removed, which saves additional space on the converter's PCB.

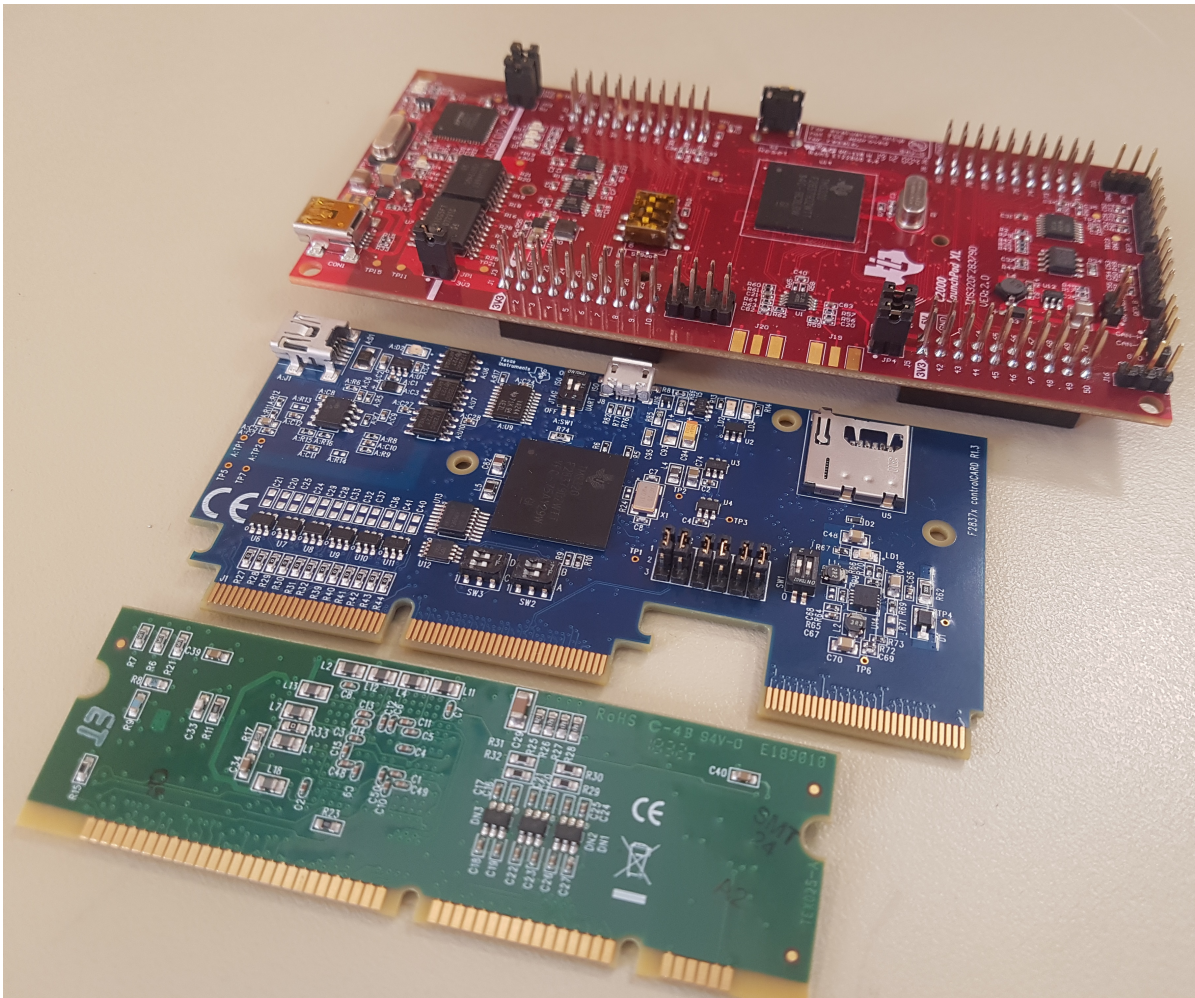


Figure 5.1: Comparison of different control hardware. F28379D-Launchpad (top) used in summer term 19 [13], F28379D-Card (middle) used in this project and F28335-Card (bottom) used in winter term 19/20 [2].

	F28388D controlCARD	F28379D controlCARD	F280049C controlCARD	F28335 controlCARD
Connector	180-pin HSEC	180-pin HSEC	180-pin HSEC	DIMM100
CPU	2 CPUs 200 MHz 925 MIPS	2 CPUs 200 MHz 800 MIPS	1 CPU 100 MHz 200 MIPS	1 CPU 150 MHz 150 MIPS
ADC	4 ADCs 24 Channels 14 MS/s	2 ADCs 24 Channels 14 MS/s	1 ADC 21 Channels 10.35 MS/s	1 ADC 16 Channels 12.5 MS/s
PWM	32 Channels	24 Channels	16 Channels	12 Channels
RAM	338 KB	204 KB	100 KB	68 KB
Flash	1536 KB	1024 KB	256 KB	512 KB
Trip-Zone Detection	yes, with integrated comparators	yes, with integrated comparators	yes, with integrated comparators	yes
Price*	274.17 €	175.07 €	109.01 €	75.97 €

*Ordering price at <https://www.mouser.de/> as of 2021-01-21.

Table 5.1: Comparison of the F28335 control card to other available control cards with a 180-pin HSEC connector. The green column marks the control card that is chosen for this project.

The F28388-Card is the most high-end but accordingly also the most expensive option. Furthermore, it is equipped with big ethernet connectors which are unnecessary for this project and take up additional space. The F280049C-Card is the cheapest option but has a different geometry than the other cards. Its larger height leads to greater space requirements in the housing and, since this vertical space can't be utilized by other components, also to a lower total power density of the converter.

For these reasons the F28379D-Card is a good trade-off between computational power, peripherals and also geometry. It is thus chosen for the converter. Figure 5.1 shows a size comparison for the control hardware of this project and previous projects. It is worth mentioning that the F28379D-Card's MCU is the same as in the F28379D-Launchpad used in summer term 19 [13] and thus that it is theoretically possible to re-use the old MCU-software. However, it is recommended to incorporate the improvements made in winter term 19/20 [2] instead.

6 Assembly of the 19/20-Converter

Due to the COVID-19 pandemic starting in 2020, the project group of winter term 19/20 was not able to build up and test the converter designed in [2]. For this reason, the task of assembling and testing that converter is passed to this project group. However, due to some technical difficulties the assembly was not able to be fully finished between the lockdown phases of 2020, hence why testing was also not possible. Pictures of the current assembly status can be seen in Figure 6.1.

In this chapter, important parts of the build up process are documented such as necessary converter design changes, as well as encountered problems and their respective solutions.

6.1 Production of the Heatsink

As the used GaN transistors are the devices with the highest estimated losses and furthermore are critically seen in terms of thermal destruction, a suitable heatsink is needed. The converter is set up in a way that the whole PCB is cooled with a water cooling system which is integrated in the housing. For the operation in the laboratory such a water cooled application seems to be elaborately. Furthermore operating the system in a closed housing comes with the drawback of not being able to measure on the board, which is totally necessary for the start-up of the board.

To overcome this problematic a heatsink is to be designed which fits the specific geometry of the PCB's bottom side with its thermal vias for cooling the mosfets and

6 Assembly of the 19/20-Converter

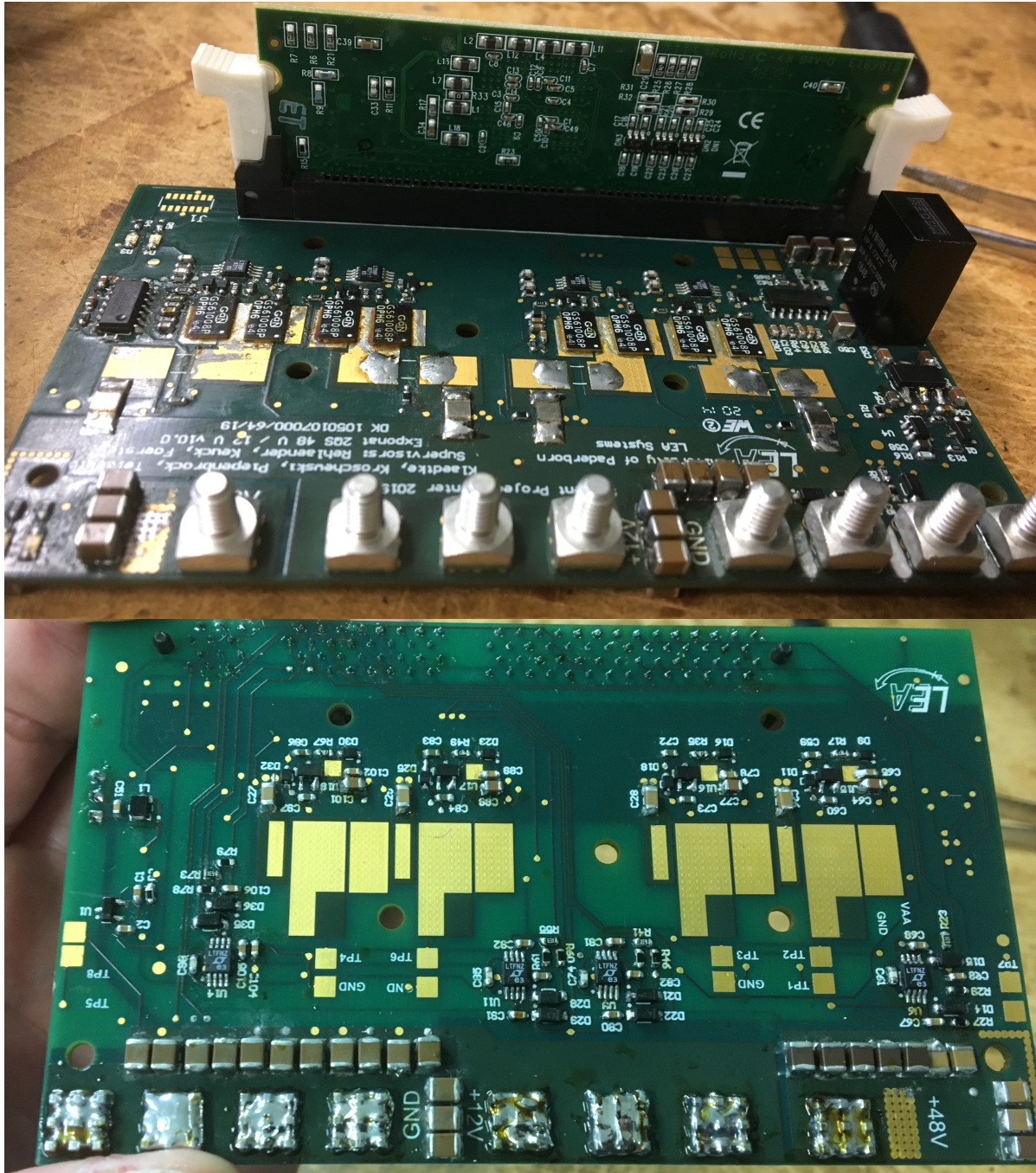


Figure 6.1: Current assembly status of the converter from winter term 19/20.

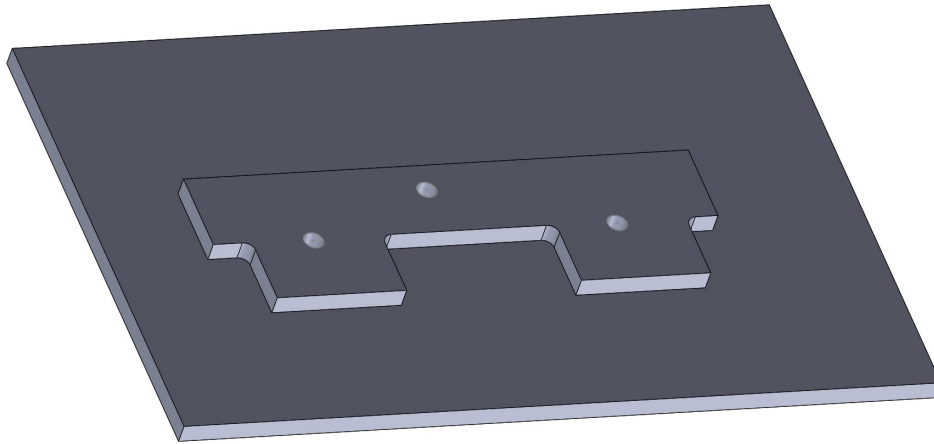


Figure 6.2: CAD model of the heatsink

the coil. The CAD model of this heatsink can be seen in Figure 6.2. The pedestal has been milled out of a heatsink blank in cooperation with the "Zentralwerkstatt" at the University of Paderborn.

The manufactured heatsink can be seen in Figure 6.3. Due to the subtractive manufacturing process with a limited drill size especially the inner corners have to be designed carefully to not block any electrical components of the PCB's bottom side.

6.2 Assembly Process

While the project group of winter term 19/20 achieved a very compact converter design, some errors were made during the layout process. These errors, as well as potential solutions, are briefly explained below so that the next project group can continue to work on the converter successfully.

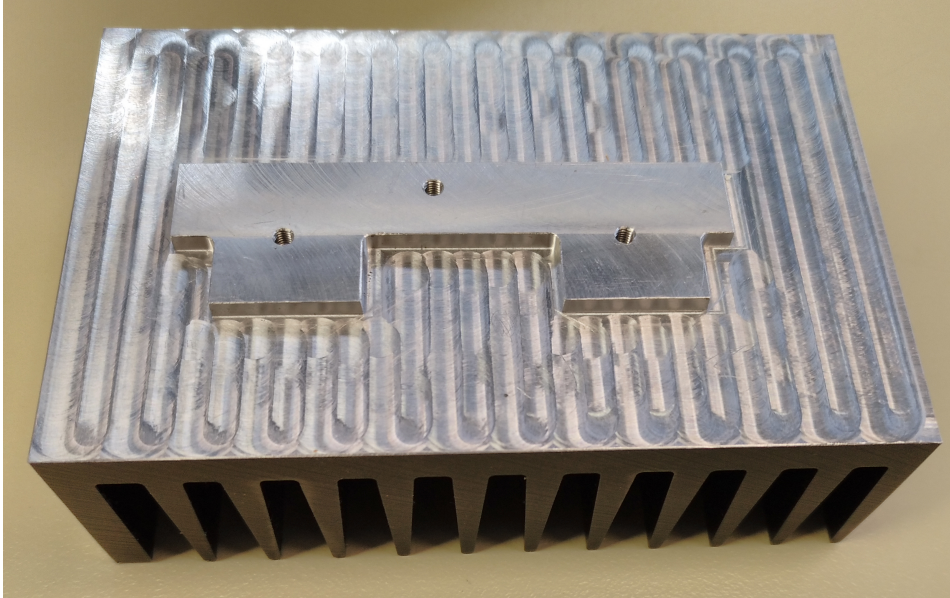


Figure 6.3: Manufactured heatsink

Soldering of GaN Transistors

A very difficult step of assembling the converter is the soldering of the GaN transistors. The GS61008P transistors used in [2] are cooled from the bottom-side, hence not only all electrical but also thermal connection pads are underneath the package, making soldering by hand difficult.

Soldering with a machine is usually an easier alternative in such cases, but is also difficult here because pads on the PCB were chosen too large for this specific transistor package, as can be seen in Figure 6.4. Usually during machine soldering with pads of the right size, the surface tension of the solder is enough to hold the component in place. But with the pads being too large, the transistor often flowed away during soldering, taking many attempts of soldering and de-soldering to guarantee a proper electrical connection, which in turn can damage the transistors. It should also be noted that, also to avoid damage during soldering, the soldering heat profile specifications of the manufacturer should be strictly adhered to.

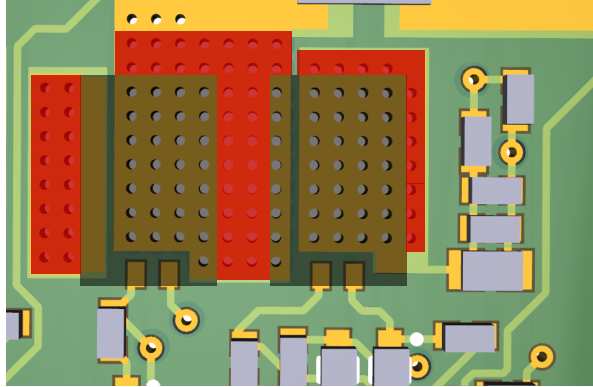


Figure 6.4: Solder pads for GS61008P GaN transistors. The black area marks the approximate component size and the red area marks where pad size could be reduced for better soldering.

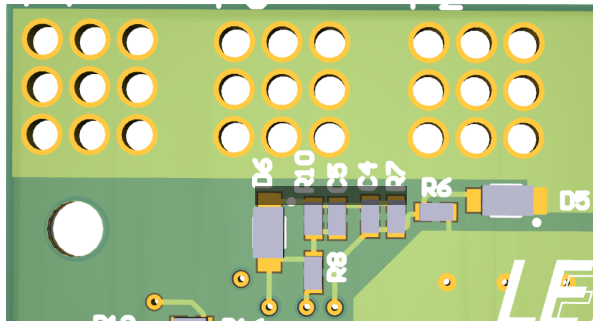


Figure 6.5: Missing ground connection. The black area marks the pads that need to be manually connected to ground.

Missing Ground Connection

During assembly, a missing ground connection in the top side of the PCB layout was noticed. The components, as shown in Figure 6.5, form voltage dividers for the measurement of converter input and output voltage. Since a floating potential not only gives wrong voltage measurements for the control algorithm but can also possibly damage the control hardware, the missing ground connection needs to be established manually for the converter to be safely operated.

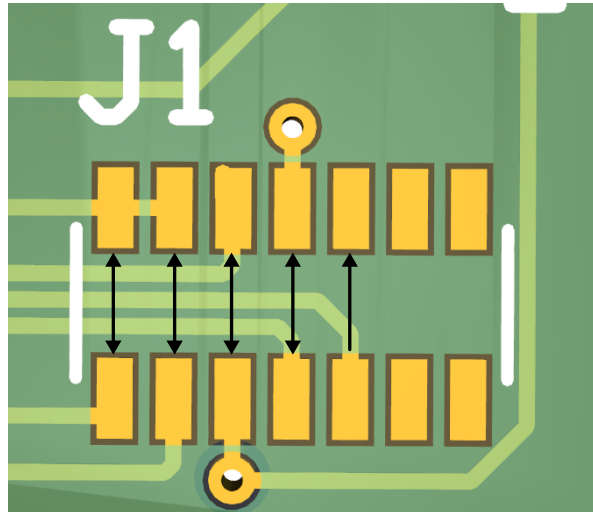


Figure 6.6: Mirrored JTAG connector pads. The arrows show which pad have to be swapped to ensure a proper connection.

Mirrored JTAG connector

To debug the control code during converter live operation, a JTAG connection needs to be established between the control hardware and the machine running the debug software. While soldering the necessary connector, it was noticed that the pads were accidentally designed with having a male connector pin layout in mind. Since the needed connector is actually female, the pads on the PCB are essentially mirrored. While some of the pads are not connected, the others thus need to be mirrored again, as suggested in Figure 6.6, to achieve proper operation of the JTAG interface.

7 Abstract

A fully new design for a 2 kW bidirectional DC-DC converter is done, based on the results and experiences from previous projects designing a 1 kW converter using GaN MOSFETs. This new design features a new inductor topology, which is iteratively improved based on FEM simulations, and silicon instead of GaN transistors, which are chosen carefully based on their expected power losses and the resulting junction temperature.

A new schematic, auxiliary circuitry and PCB layout are designed based on previous experiences and new control hardware is chosen to replace the old one because of availability issues. Furthermore, the assembly of the latest iteration of the old 1 kW is started during this project but could not be completed, again because of the COVID-19 pandemic.

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