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Student Project

in partial fulfillment of the requirements for the degree of
Master of Science
in Electrical Engineering

REDESIGN OF A 1 KW AUTOMOTIVE DC-DC CONVERTER FOR INCREASED POWER DENSITY

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1 Introduction

In many automotive applications it becomes common to use an additional 48 V wiring system besides the classical 12 V wiring system. Especially in high class vehicles with many electrical devices the power supply of them with the 12 V system would lead to a high current, and thus cables with a large surface area would be needed. This would increase the weight of the vehicle. Since decreasing the weight of the vehicle plays a key role in reducing the energy consumption it is beneficial to have the additional 48 V system for electrical components, with high energy consumption. In many cases this technique is realized with two separated batteries one for the 12 V system and one for the 48 V system. For weight reasons it is advantageous to avoid the use of the second battery or to use a smaller 12 V battery at least. Instead of the second battery it is also possible to implement the 12 V system with a buck converter and only one 48 V battery. This buck converter is developed over the last two years in many student projects which all had the aim to increase the efficiency and the energy density of the converter.

1.1 Task Description and Starting Point

The main goal of the project this semester is to increase the power density and at the same time keep the efficiency as in the former version of the converter. The starting point is a four times interleaved converter [1] with the following technical specifications:

- Maximum efficiency $\eta_{\max} = 97\ \%$
- Efficiency at 1 kW $\eta_{1\ \mathrm{kW}} = 94\ \%$

- Volume of the converter $V = 0.73\ \mathrm{dm}^3$
- Power density of the converter $\frac{P}{V} = 1.37\ \frac{\mathrm{kW}}{\mathrm{dm}^3}$

The latest design still leaves some space for improvements, especially for the power density. In particular a large control card is being used so that the size of the housing is limited to the size of the controller. The main task was to integrate a new smaller controller directly on the PCB and to implement the control strategy on this controller.

2 Comparison and selection of an alternative control card

The F28379D-Launchpad previously used for controlling the converter offers high performance and utility at the cost of taking up a lot of space. To reduce the converter's volume and thus increase its power density, alternatives are being sought. Mainly the F28379D-Launchpad's second CPU and on-board programming interfaces are considered unnecessary for the current use of the converter.

A good alternative are control cards that can be programmed via a docking station and therefore do not require any additional hardware for an on-board interface. Figure 2.1 shows a control card next to the F28379D-Launchpad. The main advantage of the control card is clearly its size but also its connector. All three control cards selected for comparison have a DIMM100 connector which gives a few advantages compared to the launchpad's connectors.

The DIMM100 connector allows the control card to be placed upright and next to the coils' ferrite. This placement saves a lot of space and offers additional options for the housing concept which is described in more detail in chapter 3.

Furthermore, the DIMM100 connector is a single connector which concentrates all input and output signals of the controller in a single place, so that the ports are not distributed over the entire circuit board as is the case with the F28379D-Launchpad. This allows the traces for power and signal flow to be spatially separated from each other, as described in more detail in chapter 4.

Additionally, the possible cooling strategies for the GaN semiconductors are severely

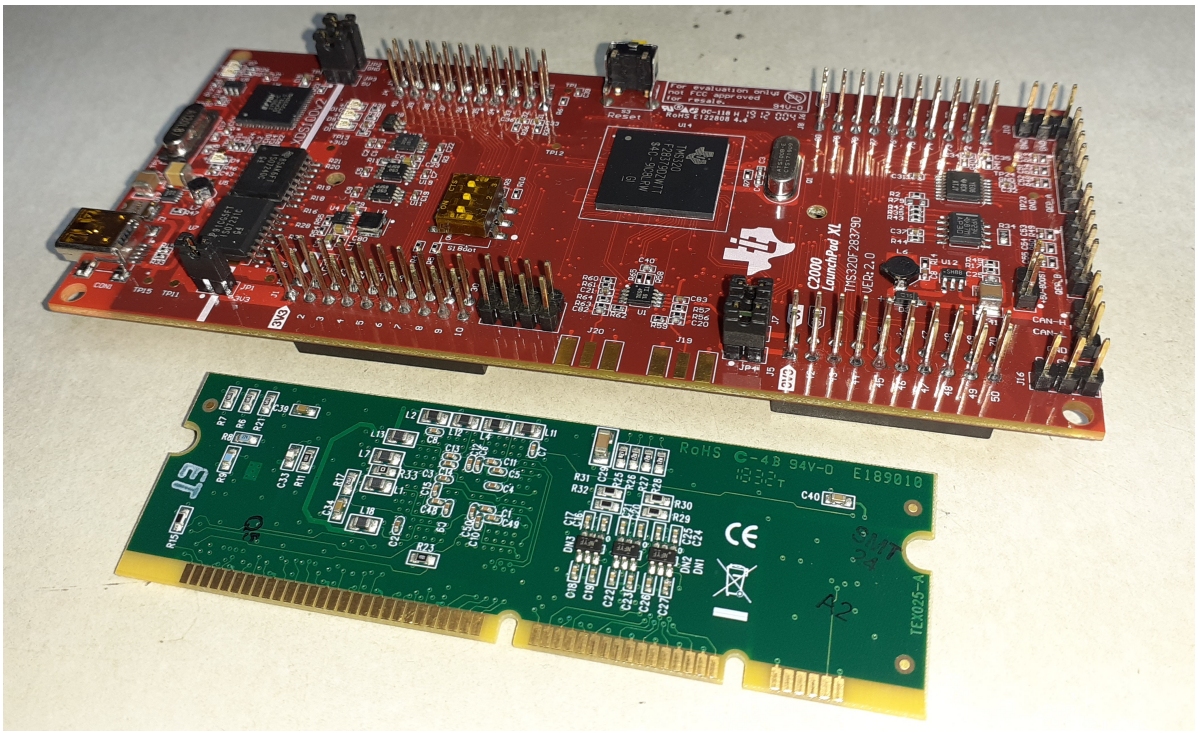


Figure 2.1: A F28335 control card (in front, green) next to the F28379D-Launchpad (red).

	Delfino F28379D LaunchPad	Delfino C28343 controlCARD	Piccolo F28069 controlCARD	Delfino F28335 controlCARD
Connector	2x40 PIN BoosterPack	DIMM100	DIMM100	DIMM100
CPU	2 CPUs 200 MHz 800 MIPS	1 CPU 200 MHz 200 MIPS	1 CPU 90 MHz 180 MIPS	1 CPU 150 MHz 150 MIPS
ADC	4 internal ADCs 24 Channels 14 MS/s	2 external ADCs 12 Channels 2 MS/s	1 internal ADC 16 Channels 3.45 MS/s	1 internal ADC 16 Channels 12.5 MS/s
PWM	24 Channels	18 Channels	16 Channels	12 Channels
RAM	204 KB	260 KB	100 KB	68 KB
Flash	1024 KB	0 KB (non-Flash technology)	256 KB	512 KB
Trip-Zone Detection	yes, with integrated comparators	yes	yes	yes

Table 2.1: Comparison of the F28379D-Launchpad and the selected control cards. The green column marks the control card that is chosen for this project.

limited by the position of the F28379D-Launchpad below the circuit board. The new control cards, on the other hand, allow for the use of a bottom cooled strategy, which is described in chapter 4.2 and thermally simulated in chapter 5.

Important features of the three control cards selected for comparison and of the F28379D-Launchpad are compared in table 2.1. Since all cards have slightly different architectures and therefore the code has to be rewritten for each card, the cards cannot all be tested and compared in practice. The selection is therefore made solely based on properties shown in the table. Of the cards shown, the F28335-Card is chosen because it has a similar clock frequency to the F28379D-Launchpad and, compared to the F28343-Card, has significantly faster and, more importantly, internal ADCs.

But since the F28335-Card generally works noticeably slower than the F28379D-Launchpad, its code still has to be rewritten entirely and optimized for the new control

card. A detailed description of the new hardware configurations and the rewritten software can be found in chapter 7. The changed processor frequency also influences control behavior. Therefore, a re-dimensioning of control parameters is necessary, which is described in chapter 8.

Furthermore, a change of the control hardware is accompanied by the loss of some important utility features offered by the old F28379D-Launchpad. Since some of these features are used for security measures for the converter, alternatives must now be implemented externally on the converter's circuit board. A description of the circuitry required for this can be found in chapter 6.

3 Housing Concept

In the following chapter a housing concept is presented. This concept provides an appropriate protection of the PCB, the magnetic components and all other sensitive components against the penetration of water or dust. Moreover, during the development process the housing was designed to enable the highest possible energy density.

3.1 Requirements

Due to the usage of the converter in an automotive application the housing needs to fulfil at least the requirements of the IP6K6K norm [2] which prescribe that the housing needs to be dust-tight and provides a fully protection against contact. This norm also requires a protection against temporary flooding of water.

3.2 Mechanical Construction

The housing consists of two separate parts. The first part is the side together with the liquid cooling system on the bottom. In the side part are three round drills which are later used to direct the GND, 48 V and 12 V through a rubber seal via copper rails out of the housing (see fig. 3.1). This concept allows a water and dust-tight connection of all external connections. On the bottom side there is an increase of the surface for the cooling ribs and for small drills parallel to the bottom for guiding the cooling water around the cooling ribs. The cooling ribs are placed directly under the four half-bridges

of the converter, which are the main source of heat losses on the PCB (see chapter 5). The PCB is mounted in the housing by five drills. For the three drills in the middle rubber spacing bolts are used to ensure a tight fitting of the ferrite.

The second part is the top cover. On the bottom side of this part there are two steps (see fig. 3.2(b)). Between the first one and the side walls a rubber seal will be placed to ensure a waterproof closing of the housing. With the second step the ferrite is pressed onto the rubber spacing bolts such that there is a thermal connection between the ferrite and the cover.

3.3 Cooling

Since the converter is used in the engine space of a car where a liquid cooling system exists it is common to use this system for the cooling of the converter. To enable a cooling of the transistors and the PCB over a large surface area it is decided to use bottom cooled transistors instead of top cooled. The use of this transistors makes it possible to cool the whole PCB and the transistors through the liquid cooling system of the housing.

The other main source of heat is the magnetic core of the coils within the ferrite; therefore, it is necessary to cool the ferrite. This is realized by a thermal connection of the housing cover with the ferrite. To ensure a safe contact between cover and ferrite rubber spacing bolts are used on the bottom side of the ferrite (see fig. 3.2).

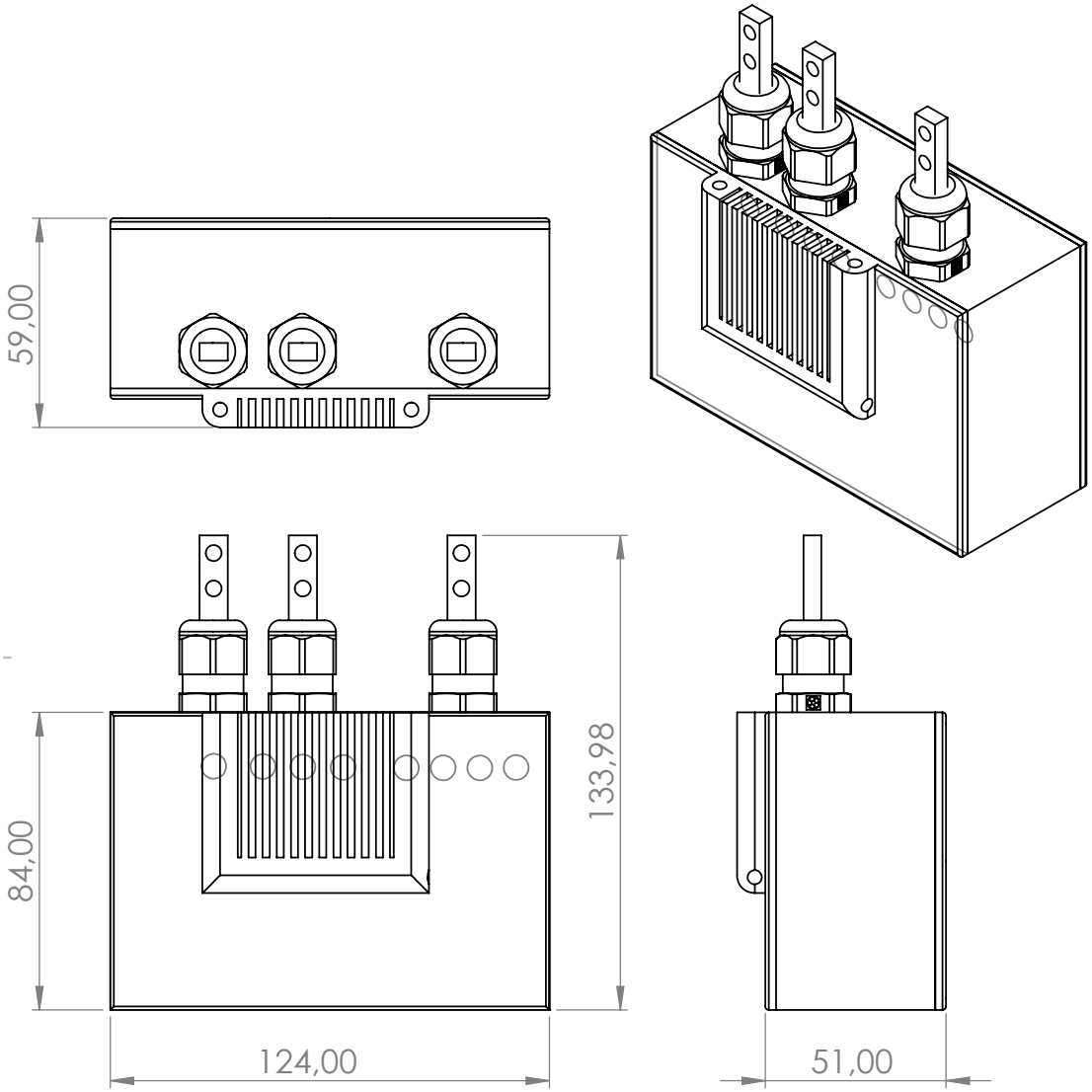
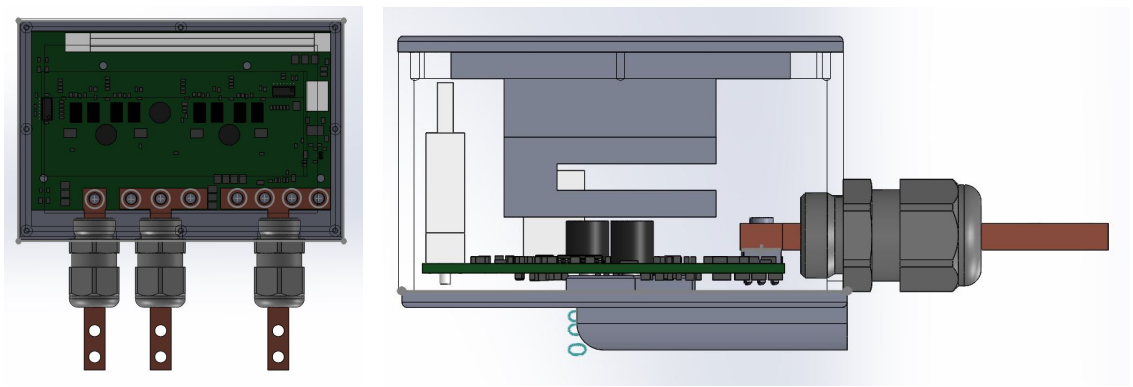


Figure 3.1: Housing with all components.



(a) 3D top view.

(b) 3D side view.

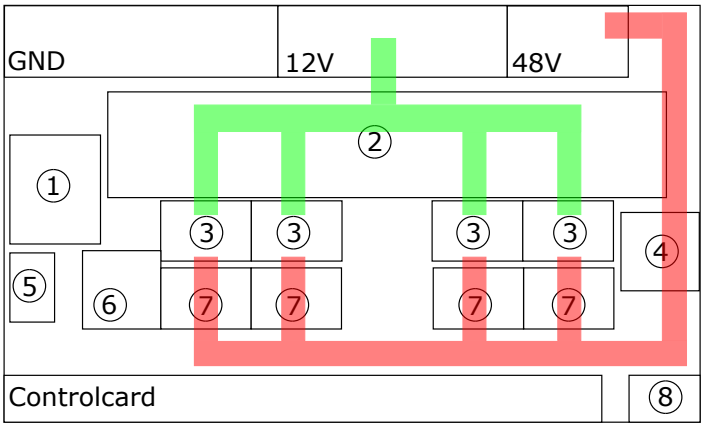
Figure 3.2: Internal view of the housing

4 PCB Design

One aim for the new design of the printed circuit board (PCB) is to increase the power density. Besides this the new design should offer an easy connection of the load and the external power source. To comply with these requirements, most of the old layout was redesigned.

The main changes in the new design are the integration of a new controller directly on the PCB and the usage of eight bottom-side cooled transistors instead of twelve top-side cooled.

Figure 4.1 shows an overview from the top side of the new PCB layout. The main current paths are marked with different colors red for 48 V and green for 12 V. The ground potential is conducted over a large area via layer 2 of the PCB.



1 : 5 V Power supply
2 : Ferrite with coils
3 : Half-bridge circuits
4 : Window-comparator 1
5 : 3.3 V Power-supply
6 : Window-comparator 2
7 : Gate-driver circuit
8 : JTAG-interface

Figure 4.1: Overview plan

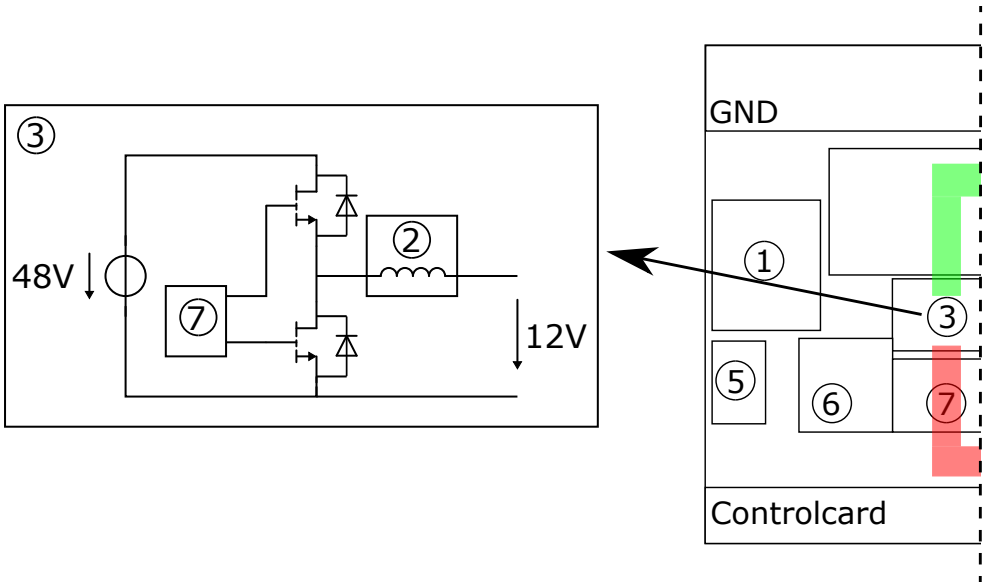


Figure 4.2: Schematic structure of the half-bridge.

4.1 Integration of the new Control Card

At the beginning of the project the decision was made to use a new compact controller since the old one is to large and offers a lot of functions, which are not used for the converter control. The new control card is connected to the PCB via a DIMM100

socket. The connections inside the white box J2 in figure 4.3(b) are for this socket.

To integrate the socket on the PCB it was necessary to design the layout such that the connections for the load and the external power supply are on one side. Such a design is also advantageous for the housing because it requires only drill holes on one side for the connections.

The usage of the compact control card offers some more advantages. In the old design the controller was the largest component, so decreasing the size of the PCB would not decrease the volume of the converter. With the new control card, the only limit in the size of the PCB is the length of the DIMM100 socket. This makes it possible to reduce the surface of the PCB around 14.34 % from 91 cm^2 to $77,95$ cm^2. The volume of the converter with the housing is reduced by 16.44 % from 0.73 dm^3 to 0.61 dm^3. The new smaller volume of the converter will lead to a theoretical power density of

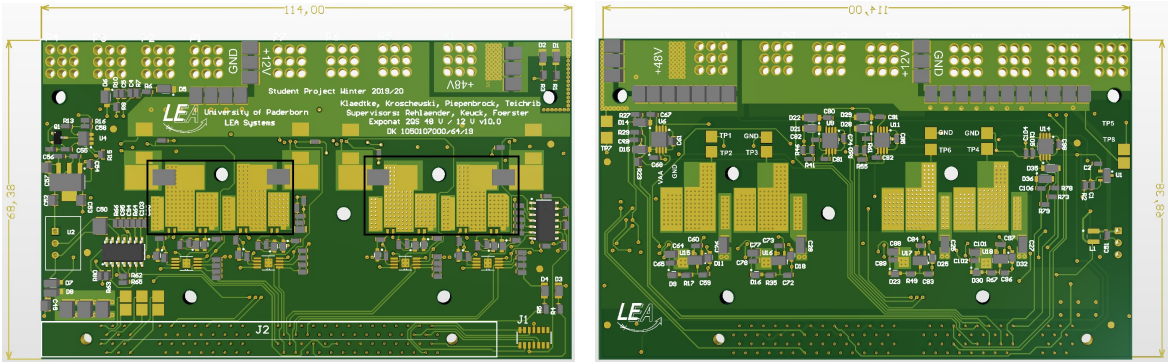
$$\frac{P}{V} = 1.64 \ \frac{\text{kW}}{\text{dm}^3} \tag{4.1}$$

which is an increase of 19.66 % compared to the last version of the converter. Clearly this value has to be verified experimentally during the commissioning of the converter.

The old controller was connected to the PCB via four sockets on the bottom side which are no longer needed for the current control card. So, with the new design the bottom side of the PCB is not covered by the controller which makes it possible to use bottom-side cooled transistors and to cool them by a large surface area on the bottom side.

4.2 Bottom-side cooled Transistors

Due to the new compact design of the housing and the PCB as shown in figure 3.2 the ferrite is now placed directly over the transistors, thus a top-side cooling of them is not possible. But as described in the previous section, the new design also offers a direct thermal connection on the bottom side of the PCB to the liquid cooling system



(a) Top side

(b) Bottom side

Figure 4.3: PCB layout

of the housing. To transfer the heat losses of the bottom-side cooled transistors to the bottom-side of the PCB thermal vias are placed in between. To ensure that it is still possible to solder the transistors even with vias underneath them, filled and capped vias are used. The vias inside the black box in figure 4.3(a) are filled and capped.

To achieve the best possible thermal conductivity through the vias an optimization of the effective copper-filled area is being used. The optimization is based on a modified consideration used in [3]. Because of the space limiting drain and gate pads the theoretical optimal orthocyclic arrangement of the vias cannot be implemented usefully and a primitive checkerboard pattern must be used. As a result, the optimal diameter for the vias is 0.5 mm (see figure 4.4). Also, there are only small deviations of the effective copper-filled areas between the diameters 0.4 to 0.7 mm. Because a small drill size allows a higher flexibility in designing 0.4 mm is chosen as the best compromise. Additionally, in an industrial background it can be considered keeping costs during the manufacturing process at a minimum by changing drill sizes as rare as possible.

In the old version of the layout two low-side transistors are used for each half bridge in order to reduce the conduction losses. During the redesign of the PCB a problem with the second low-side transistor occurred. It was not possible to connect the source of the second low-side transistor to the gate driver output with a small loop. The problem was that the driver signal always has to be routed next to a copper plane where the potential jumps from 12 to 48 V with the switching frequency, which may cause errors

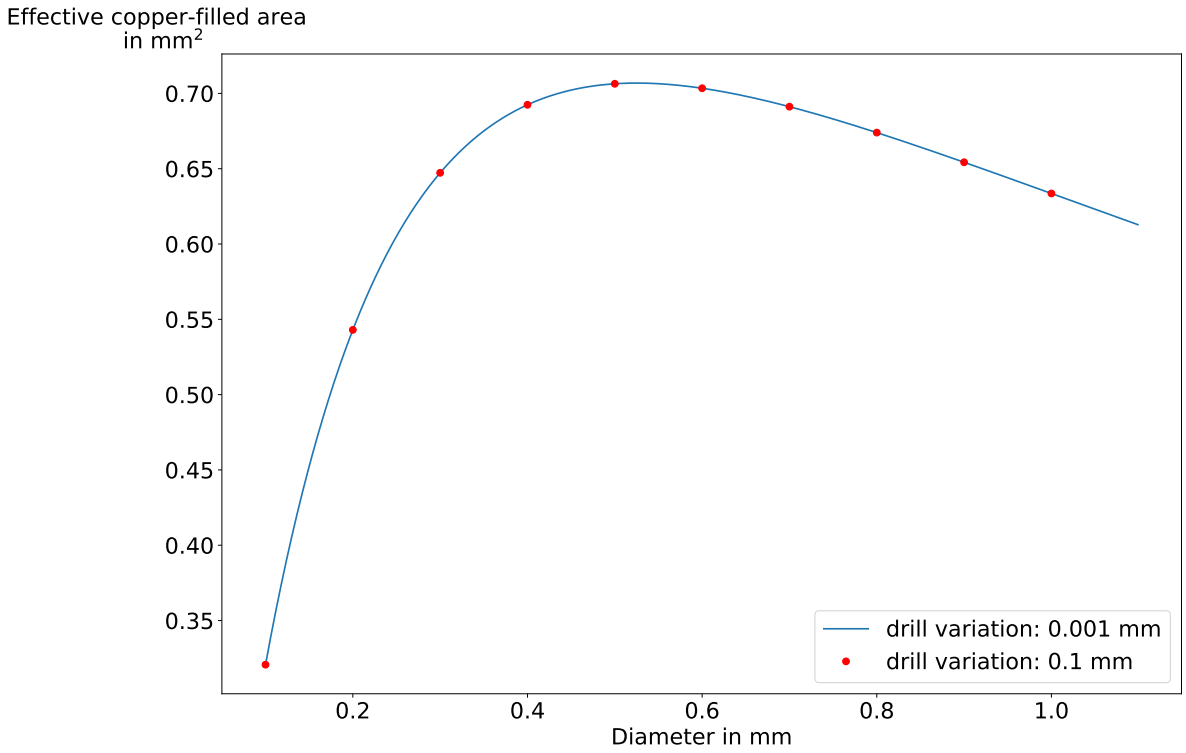
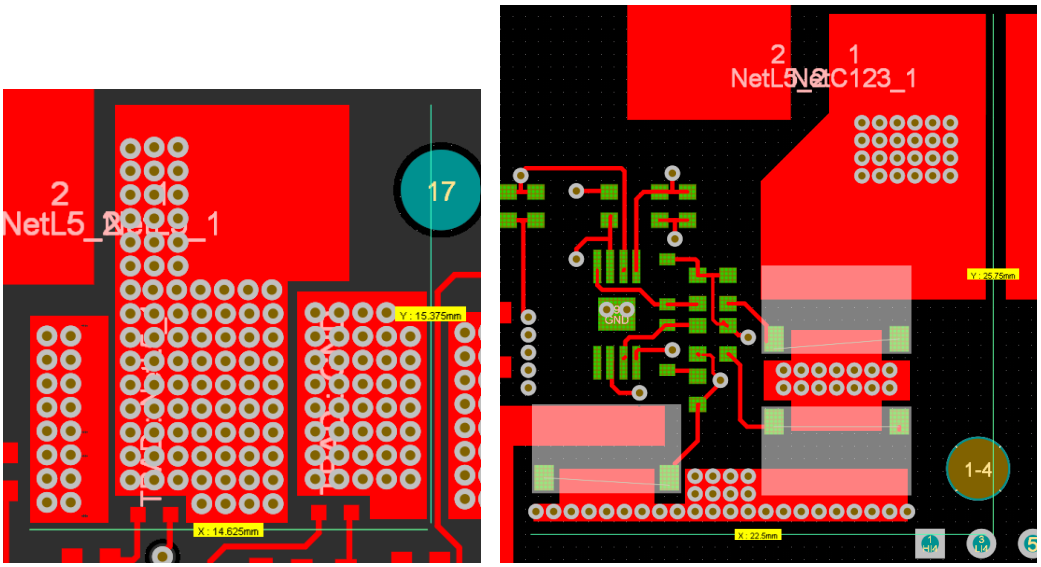


Figure 4.4: Optimization of the thermal vias

in the control of the transistor. The usage of only one low-side transistor increases the conducting losses but on the other hand it decreases the switching losses and it is possible to further decrease the size of the PCB [4]. As constituted in figure 4.5 the lengths of the high current conducting traces have been reduced to a minimum. All in all, the advantages outweigh the disadvantages and it is necessary to only use one low-side transistor.



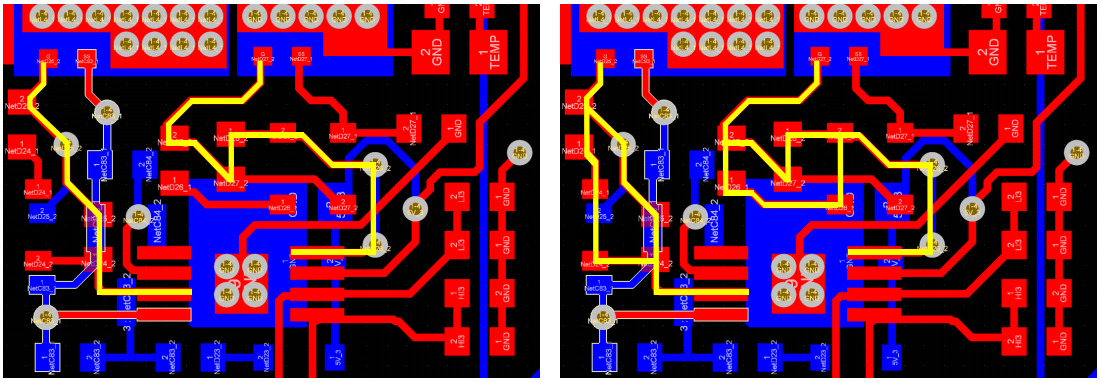
(a) Layout of the current converter (b) Layout of the old converter

Figure 4.5: Comparation layout of the GaNs

Due to the comprehensive changes in the way of placing the GaNs, also the routing of the driver circuit has been built up in a completely new way. The spanned area of the path from the driver to the gate during loading and unloading should be designed as small as possible.

4.3 Comparator Circuits

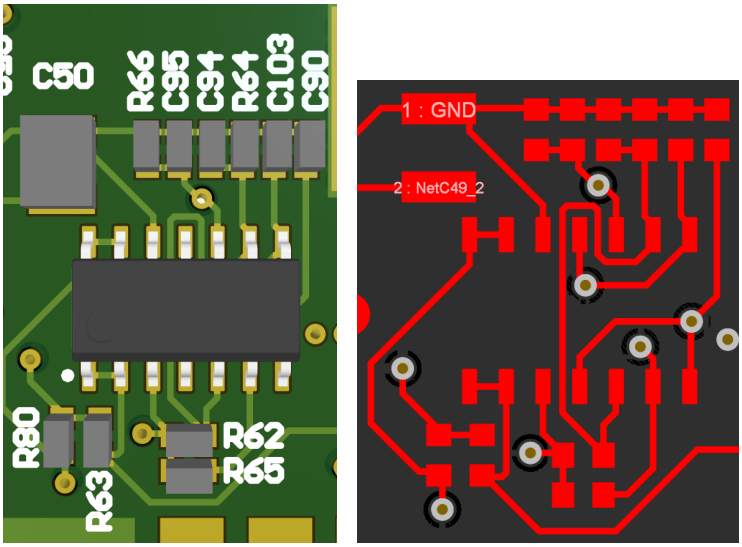
As specified more detailed in section 6.2 external window comparators are needed for every rail. The integration of two 14 pin LMV339 quad-comparators, the required



(a) Gate loading path (b) Gate unloading path

Figure 4.6: PCB layout of the driver circuit

resistors and capacitors into the PCB layout is shown in figure 4.7.



(a) Comparator circuit 3D (b) Comparator circuit 2D

Figure 4.7: Comparator circuit

5 Thermal Simulation

Because of the Corona Crisis the DC-DC converter could not be put into operation. In this chapter a theoretical evaluation of the unavoidable negative effects of non-ideal power parts is presented. The analytically calculated losses are not representative for an efficiency analysis. Here, only the thermally stressed components, as there are especially the GaN semiconductors and the magnetics (ip. ferrite cores), are considered. Thermal stress is the result of high-power losses in a small volume or in a model on a small surface combined with a bad cooling environment.

Due to the power losses in table 5.2 the components are heated and must be cooled. In particular the GaN semiconductors are critically worth being protected from overheating. Also, the ferrites and the FR-4 board material are specified with maximal operating temperatures. Although the temperature of decomposition is stated as 310 °C, the FR-4 comes with a glass transition temperature of at least 110 °C [5]. In order to the increasing forward resistance of the transistors at higher operating temperature, the optimal operating temperature is the lowest possible [6]. In case of the ferrites the dependency of the optimal operating temperature is much more complicated. As shown in the datasheet, the temperature of the ferrite should be considered in the range of 80 °C to 120 °C. [7]

Material	**max. operation temperature**
GaN	150 °C [6]
N95	220 °C [7]
FR-4	110 °C [5]

Table 5.1: Maximum operation temperatures of the thermal critical materials

Losses	$P_{\mathbf{loss}}$ **in** W	**Calculation**	**Conditions**
Low-side forward	18.2	$4 \cdot I^2_{\mathrm{RMS,LS}} \cdot R_{\mathrm{DS,on}}$	$R_{\mathrm{DS,on}} = 0.014\ \Omega$ at approx. 115°C [6]
Low-side dead time	3.33	$8 \cdot U_{\mathrm{SD}} \cdot I \cdot f_{\mathrm{s}} T_{\mathrm{death}}$	$U_{\mathrm{SD}} = 2.5$ V, $f_{\mathrm{s}} = 200$ kHz, $T_{\mathrm{death}} = 40$ ns [6]
High side forward	4.8	$4 \cdot I^2_{\mathrm{RMS,HS}} \cdot R_{\mathrm{DS,on}}$	$R_{\mathrm{DS,on}} = 0.011\ \Omega$ at approx. 90 °C [6]
High side switching	3.53	$4 \cdot f_{\mathrm{s}} \cdot (E_{\mathrm{on}} + E_{\mathrm{off}})$	$E_{\mathrm{on}} = 2.8$ µJ, $E_{\mathrm{off}} = 1.6$ µJ [6]
Magnetics	10	[4]	

Table 5.2: Dissipated power assigned to the thermal critical components

5.1 Simulation Model

The used simulation model is a very simplified CAD model drawn in Solidworks and imported in the simulation environment ANSYS. With the help of an FEM simulation the model is to be examined in a static thermal analysis. The corresponding power losses from table 5.2 are being imprinted as constant heat flux into the four low-side and the four high-side transistor pads. Beneath the copper pads the thermal vias are modeled by an orthotropic material which has a maximal thermal conductivity in z-dimension. The thermal resistance of the GaN semiconductors is not modeled in the FEM simulation, which must be considered for computing the transistor junction temperature. For electrical isolation a thermal interface material is placed between the PCB and the extruded aluminum socket. As the water-cooling system is being assumed to work ideally, a temperature of 60 °C can be provided as constant to the bottom-side of the housing.

Additionally, the top of the ferrite is assumed to be constant at 60 °C because of the large area connection to the housing and the low power flux densities (seen in later simulation results, see figure 5.5). For reasons of efficiency concerning the FEM simulation the magnetic part is being modeled by a cubic design. Nevertheless, the distances of the air gaps and the size of the conducting surfaces are quite the same compared to the cylindrical original part. The windings around the ferrite core are assumed to be one block of copper. The material in between the ferrite core and the copper windings is being assumed to be Kapton tape with its specific conductivity. The heat flux is

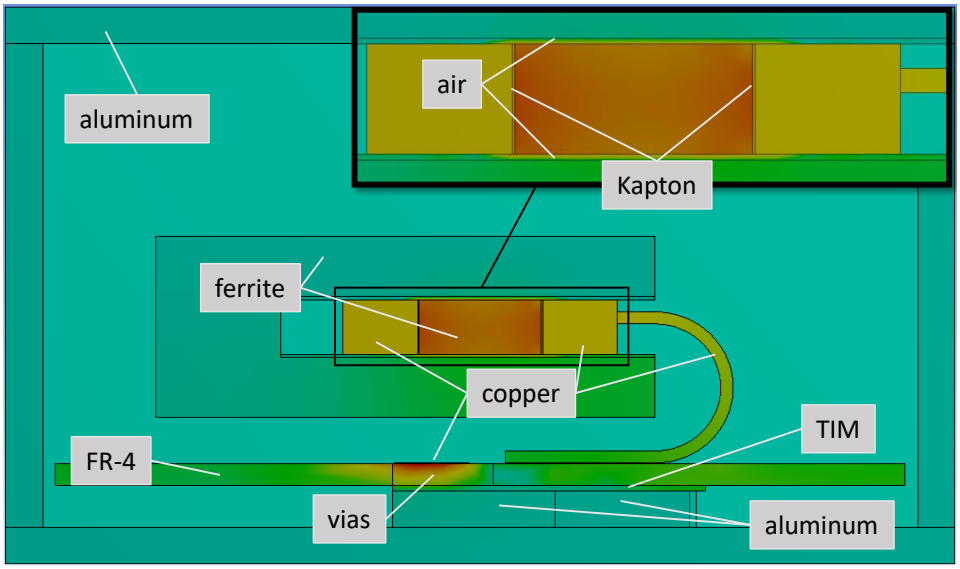


Figure 5.1: Material assignments to the simplified CAD model

imprinted into these four sides of the ferrite core because as magnetic simulations from further project groups show, the main losses are caused in the margin area of the core [4]. Because of limiting software licenses, there is only one of the four coils modeled in the simulation.

5.2 Resulting Temperature and Heat Flux: GaNs

As the most important result the junction temperature of the GaN semiconductor with its inner thermal resistance of 0.55 K/W can be estimated to 111.5 °C, whereas the maximal operating temperature is stated as 150 °C [6]. Assuming the whole power losses of the GaNs are dissipated by one path into the bottom of the housing an equivalent circuit analogous to figure 5.2 can be examined. According to the temperature differences across each component there can be calculated thermal resistances as the quotient of temperature difference and conducted power of each component.

The main temperature differences are caused by the heat conduction through the thermal vias and the thermal interface material with 26.0 and 20.3 K. Out of that

Component	λ **in** W/(m K)	**Realization**
Housing	237.5	Aluminum: 3 mm, bottom-cooled (60 °C)
TIM	5	Bergquist GAP Pad 5.0
Vias	$\lambda_z = 17.5$	Orthotropic material (λ_x, $\lambda_y = 0.294$ W/(m K)), 130 vias 1/cm^2, 25 µm copper sleeves
PCB	0.294	1.76 mm thickness
GaN pads	400	Copper: 3 mm x 6 mm x 70 µm
Ferrite	4	Cores: 10 mm x 10 mm x 4.5 mm
		Yoke: top-cooled (60 °C)
Air gaps	0.026	Air: 0.25 mm above and below the ferrite core
Kapton	0.12	Isotropic Material: 0.1 mm between the ferrite core and the copper
Windings	400	Copper

Table 5.3: Specifications of the CAD model used in the FEM simulation

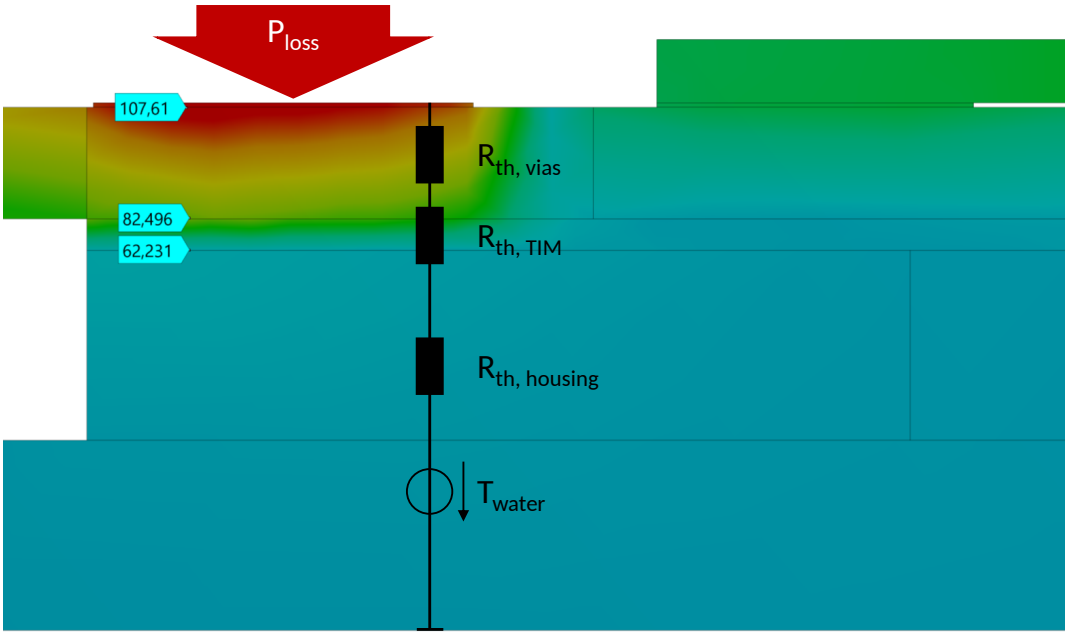


Figure 5.2: Cutting plane - temperature distribution in °C of low-side GaN - Thermal equivalent circuit

Component	**max. Temp. in** °C	ΔT **in** K	**eff.** $R_{\mathbf{th}}$ **in** K/W
Low-side GaN (junction)	111.5	3.0	0.55 [6]
Vias	108.5	26.0	4.7
TIM	82.5	20.3	3.7
Housing (socket)	62.2	2.2	0.4
Water (liquid cooling)	60.0	-	-
High-side GaN (junction)	84.5	-	0.55 [6]

Table 5.4: Results of the FEM simulation

thermal resistances of 4.7 and 3.7 K/W result for imprinted power losses of 5.5 W per low-side GaN. While comparing this $R_{\mathrm{th,vias}}$ (see table 5.4) calculated from the simulation to a simple resistor model using the surface of the imprinted heat flux, it can be figured out that the theoretical thermal resistance ($R_{\mathrm{th,theo.}} = 5.6$ K/W, cf. equation 5.1) is larger than the result of the simulation. The difference can be explained by heat spreading effects that are obviously not calculated in a theoretical, one-dimensional model.

$$R_{\mathrm{th,theo.}} = \frac{h}{\lambda A} \tag{5.1}$$

The effect of heat spreading can also be noticed in figure 5.3 where the thermal flux densities are emphasized by colors. It can be seen that the dissipated power is distributed not only vertically but also horizontally in the aluminum socket. But indeed, the thermal vias' ability of heat spreading is very limited due to their small conductivity in horizontal direction. The horizontal heat transfer is here simulated as a worst-case scenario because of the PCB's neglected copper layers, which would obviously have a positive impact on enlarging the effective cooling area.

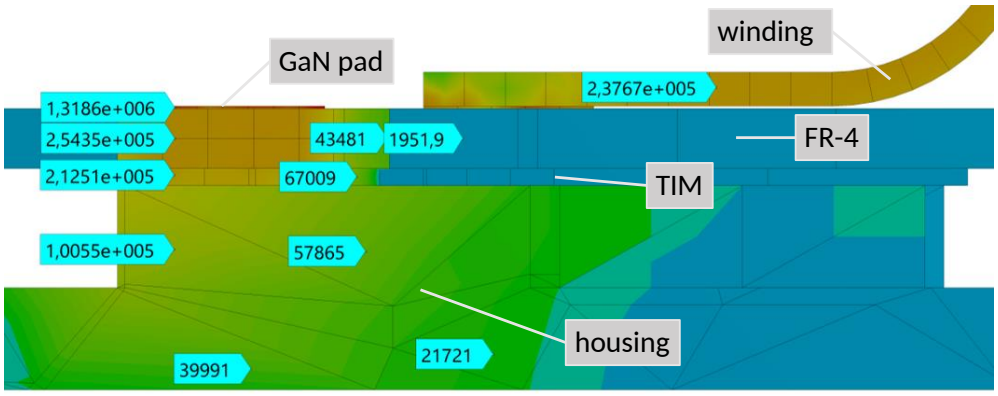


Figure 5.3: Heat flux densities in W/m^2 - Plane cut of a low-side GaN

5.3 Resulting Temperature and Heat Flux: Magnetic Components

According to figure 5.4 the maximum temperature of the ferrite core is about 100 °C and hence is in the range of a suitable operation temperature. As its boundary condition the ferrite yoke's temperature in the upper leg is about 60 °C whereas the temperature beneath the ferrite core is about 68 °C. The temperature of the copper around the core is about to be 92 °C with a temperature difference of 20 respectively 8 K to the PCB connections of the two windings. Due to the very symmetric construction it has to be assumed that the conducted power of the two windings differs from each other by a factor of 2.5.

To prove this assumption, the heat flux is being examined according to figure 5.5. Further, assuming there are three possible paths for the heat flux to dissipate the power losses out of the ferrite core, the heat can either be conducted by one of the windings or by the ferrite yoke. As the right winding is connected to thermal vias, the left winding is due to layouting reasons only soldered on a pad without thermal vias. Indeed, this construction results in an even more than 2.5 times higher heat flux density in the right winding (see 5.5). As a result, half of the totally dissipated power in the ferrite core is conducted by the right winding and about 30 % by the ferrite yoke. The resulting heat flux densities in the ferrite yoke are mainly concentrated above the ferrite core and

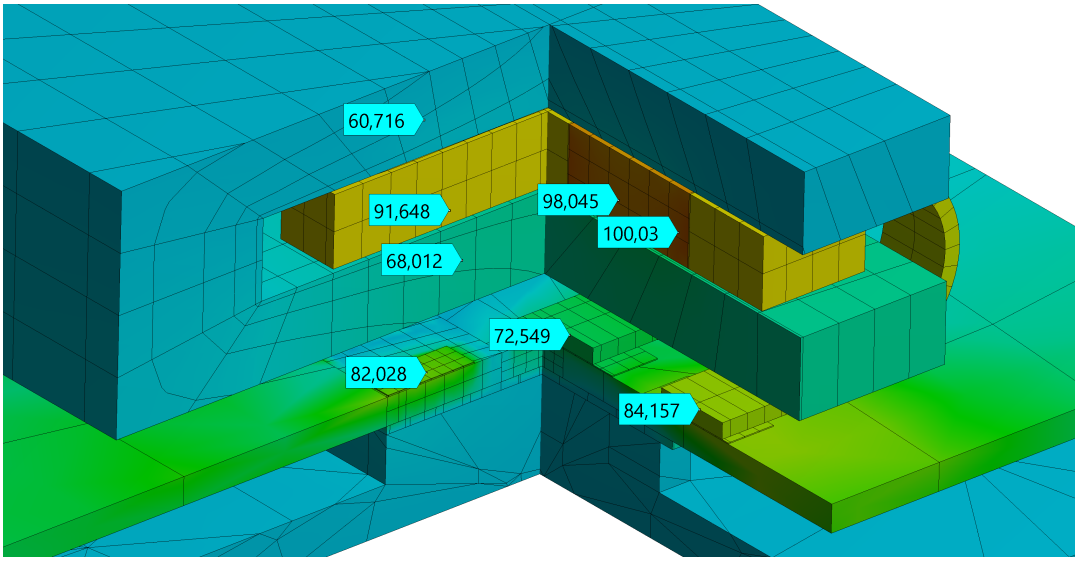


Figure 5.4: Cutting plane - temperature distribution of the magnetic component

distinctly smaller compared to the values in the windings. As mentioned in 5.1 there is only one of four windings modeled in the simulation. Because the main heat flux is being conducted by the windings and the large area connection of the yoke to the housing it is assumed that the mutual influence of the windings can be neglected.

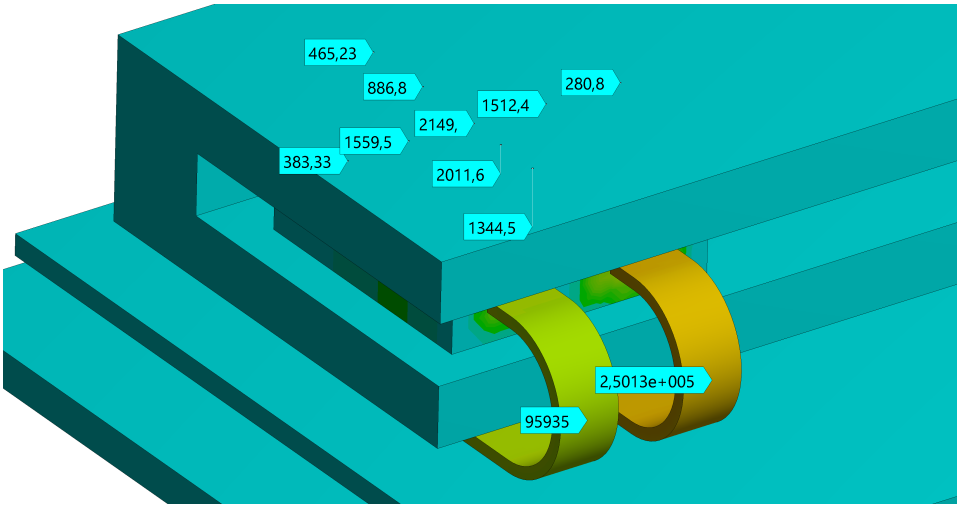


Figure 5.5: Heat flux densities in W/m^2 of the windings and the ferrite yoke

Component	**Heat flux densities in** W/m^2	**Shared power per core in** W
Ferrite yoke	max. $\approx$ 2200	0.75
Right winding (figure 5.5)	$\approx$ 250000	1.25
Left winding (figure 5.5)	$\approx$ 96000	0.5

Table 5.5: Heat fluxes in the magnetic component

5.4 Future Improvements of the Simulation

In the simulation, heat transfer by convection is being neglected because of the small sized closed system. Radiation has been taken into account but is in order to the low absolute temperatures and minor emissivity of aluminum as well negligible.

Obviously, there is an uncertainty according to the correct modeling of the magnetics. An experimental measurement could be a basis for tuning the parameters of the model. In detail, a temperature value taken from the ferrite core should be tried to be achieved with the simulation by varying the conductivity of the Kapton's geometry. With this manipulation the power distribution between the windings and the ferrite yoke can be influenced. Additionally the top of the housing should be expanded by the ferrite connection, so that the heat flux can be simulated through the housing's side walls and as a result the constant boundary condition on top of the ferrite yoke can be modeled in a more sophisticated way. To realize these changes there must be modeled all of the four magnetic windings. The modeling of the GaNs can be improved as well. In particular the PCB can be either modeled more detailed per hand or imported as an EDB file from Altium. The second variant is a bit of 'using a sledge-hammer to crack a nut' because the required mesh will be very computationally intensive. Especially modeling the hundreds of vias with their inner sleeve-structure in the size of some micrometers really would be a challenging task. As some suggestions for the hand made improvements, the main copper traces on the top and the bottom side, the connectors, shunts and the control card should be added to a new simulation model. Additionally, it is possible to divide the simulation into several parts with a more precise modelling. Then the temperature boundaries and flux transitions must be implemented and transferred from one simulation to another.

6 Protective Measures

To protect the converter in case of errors an event-based emergency shutoff has to be implemented. To achieve this the controller compares data of currents, voltages and temperature to corresponding thresholds and reacts with protective measures in case they are exceeded. As an example, in case of an overcurrent in one of the rails, that rail has to be deactivated by turning off its respective switches.

6.1 Implementation with the F28379D-Launchpad

To execute these protective measures as fast as possible both the old F28379D-Launchpad and the new F28335-Card have a trip zone unit which is able to perform the necessary actions directly in hardware thus saving as much time as possible.

A very important difference in the utility of the old and new control hardware is the F28379D-Launchpad having ADCs with integrated post processing blocks and an XBAR-architecture. While the post processing blocks can be used for a wide range of tasks, in the context of these protective measures they are only used for threshold detection. For every ADC input its corresponding post processing block can detect an upper or lower threshold excess utilizing integrated comparators. The result of this threshold detection is then stored in a specific ADC register.

With the XBAR-architecture it is possible for the controller to connect different internal signals directly in hardware. Using this architecture, the event of a threshold detection by the post processing blocks can be directly passed to an input of the trip

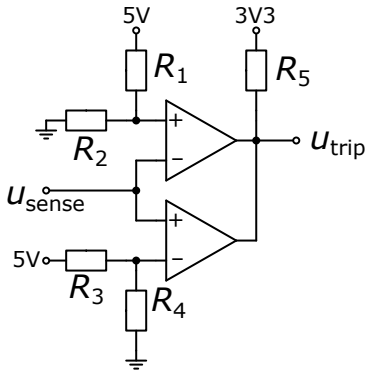


Figure 6.1: Chosen implementation of the window comparator circuit.

zone unit. Because all of this is done in hardware, very fast reaction times can be achieved for the protective measures.

6.2 Implementation with the F28335-Card

Because the F28335-Card has neither post processing blocks nor an XBAR-architecture, threshold detection and the passing of its results to the trip zone unit has to be done externally. For this reason, additional comparator circuits are needed on the converter's circuit board.

Since the converter should be able to function bidirectionally, a window comparator is needed for the current of every rail. The window comparator consists of two separate comparators of which one detects excesses of a lower and the other of an upper threshold. Their outputs are linked to one another with logical OR and the result is passed to the input of the trip zone unit.

The chosen implementation of the window comparator circuit is shown in figure 6.1. The input voltage u_{sense} is the output of a current sense amplifier and thus a function of the rail current i_{L} and the shunt resistance R_{sh} used for measurement.

$$u_{\text{in}}(i_{\text{L}}, R_{\text{sh}}) = -20 \cdot i_{\text{L}} \cdot R_{\text{sh}} + 1,6\text{V} \tag{6.1}$$

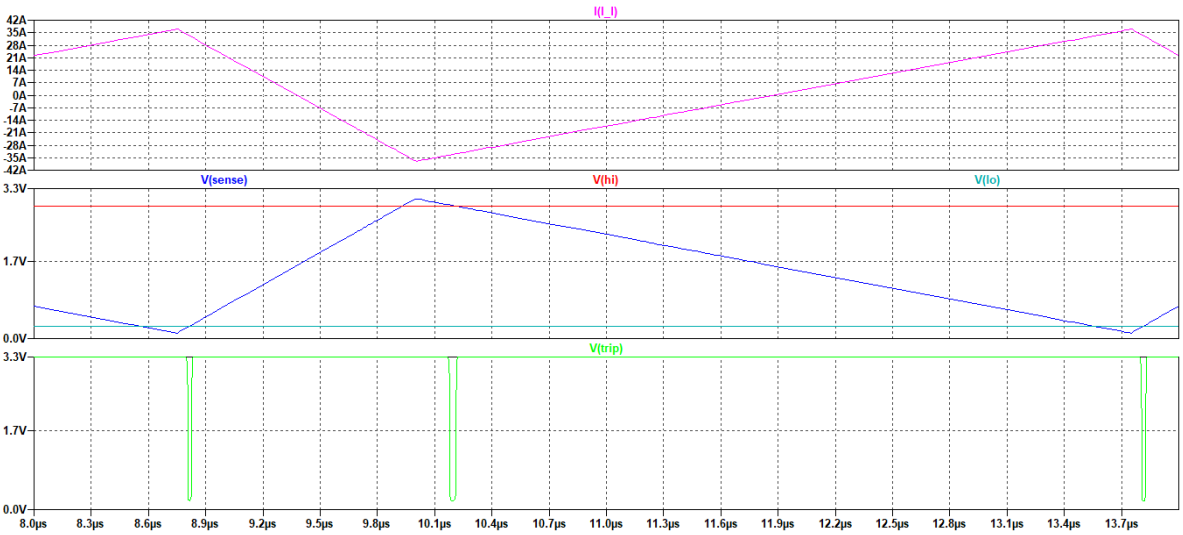


Figure 6.2: Results of the LTSpice simulation of a window comparator using the LMV339 and current limits of $+/-33$A.

The threshold levels for each comparator are given by their respective resistors R_1, R_2 and R_3, R_4. Dimensioning of these resistors can be done through converting given upper and lower current limits into voltage thresholds using equation 6.1. Using voltage divider rule, the resistances needed to achieve these voltage thresholds can then be calculated.

The comparator outputs are connected to one another and to the controller's trip input using the pull-up resistor R_5. This only works if the comparators have an open-collector or an open-drain output. In this case both comparator outputs can pull down the output voltage u_{trip} to almost 0 V resulting in a logical '0' which triggers a trip action. If none of the comparators' output is low, the voltage u_{trip} stays near 3.3 V which allows continuing normal operation of the controller.

Using 3.3 V for the trip input's pull-up voltage is done because of specifications given by the F28335-Card's datasheet. Recommended values for the pull-up resistor can be taken from the comparators' datasheet. The chosen comparator model is a LMV339 which is available in a quad-comparator package. This means a single integrated circuit with four resistors can be used to monitor two current rails, since every rail should use the same upper and lower thresholds.

Figure 6.2 shows an LTSpice simulation of the window comparator using the LMV339 and current limits of ±33 A. The window comparator's output turns low about 250 ns after the current crosses one of the thresholds.

As opposed to the currents both the converter's input and output voltage as well as the temperature are chosen not to be monitored using the trip zone unit. Since these cannot change as rapidly as the rail current both monitoring and emergency shutoff can be done in software. This saves some additional space that would have been needed for additional comparator circuits otherwise.

7 Control Board Software and Configuration

The TMDSCNCD28335 control board is equipped with a TMS320F28335 Microcontroller (F28335-MCU). The integrated peripherals like the Analog Digital Converter and the Pulse Width Modulation (PWM) module have a different design compared to the peripherals of the TMS320F28379D (F28379D) MCU used in previous semester projects. The MCU code is very hardware specific, about half the code consists of hardware configuration of MCU peripherals. Because of this the MCU code had to be written from scratch and is optimized for the F28335-MCU.

Besides the change of control parameters as described in chapter 8 the control structure as such consisting of a cascaded control scheme with an inner current loop and an outer voltage loop has not changed compared to the project of the summer term 2018 [8]. On software level the task distribution between the loop functions, the execution strategy of the loop functions and the way data is processed and organized has been optimized to enable the controller software to run on a MCU with one fifth of the processing power compared to the last MCU platform (comparison based on MIPS, see [9] and [10]).

The following section describes the configuration and operation strategy of the PWM and the ADC module. The second section focuses more on the three control loops running in different priority levels. Two special features, the use of float variables and the access possibilities during debug sessions are handled in two subsequent sections. The last section is about aspects that can be optimized in future projects.

7.1 PWM and ADC Configuration

Similar to the old code base the PWM module is working in symmetrical mode with four synchronized and phase shifted individual PWM signal generators. The deadband time is set to 7 PWM clock cycles, where one PWM clock cycle corresponds in this configuration to one CPU clock cycle. The main PWM configuration difference is a lack of the High Resolution PWM (HRPWM) functionality, which provides a better duty cycle resolution. The F28335-MCU provides this mode only for the PWM A channels, but not for the B channels (see [11, p. 7]). Because both channels are needed for the used converter topology, HRPWM cannot be used.

The shadow register mode is enabled in this configuration. Using this mode changes to the PWM counter compare registers which define the duty cycle are delayed to the next occurrence of a zero PWM counter value to prevent glitches of the PWM signal [12, p. 231]. The trip zone input is a digital input and not an analog one as in the old control board [12, p. 266]. Therefore, trip zone levels are defined by an external analog compare circuit and not set in software as described in chapter 6.2.

The ADC is fundamentally differently constructed than the ADCs used in the previous control board. It features only one actual converter with two sample and hold circuits enabling two measurements in parallel at a time. But because of the high possible sampling rate of 12.5 MSPS it can perform the needed measurements in time [12, pp. 446 sq.]. If the PWM counter of any of the four PWM signal generators reaches the period value ADC measurements will be triggered to enable regular sampling. At the here used maximum PWM frequency for four rails of 200 kHz the ADC is triggered at 800 kHz, because of the four phase shifted PWM generators.

To switch the ADC input channels between the eleven different input signals without CPU interaction a sequencer is used. The sequencer is programmed with a sequence of external analog input signals which will be multiplexed to the ADC input channels on each measurement without further CPU interaction [12, p. 463]. In this particular configuration after triggered by a PWM generator the ADC sequencer performs two double measurements resulting in four single measurement values.

7.2 Loop Functions

During converter operation tasks are executed in three loop functions with different priority and call strategies and rates, as illustrated in figure 7.1. The current loop function is executed in highest priority triggered by the ADC, followed by the voltage loop function executed in medium priority and triggered by a CPU timer. Both functions are interrupt service routines (ISR). A background loop is active during the rest of the CPU time and has low priority, it runs in the main function context.

Execution times of the various loop functions are measured using a Saleae 24 MHz logic analyzer by enabling a general-purpose input output (GPIO) pin on function entry and disabling it directly before the function exits.

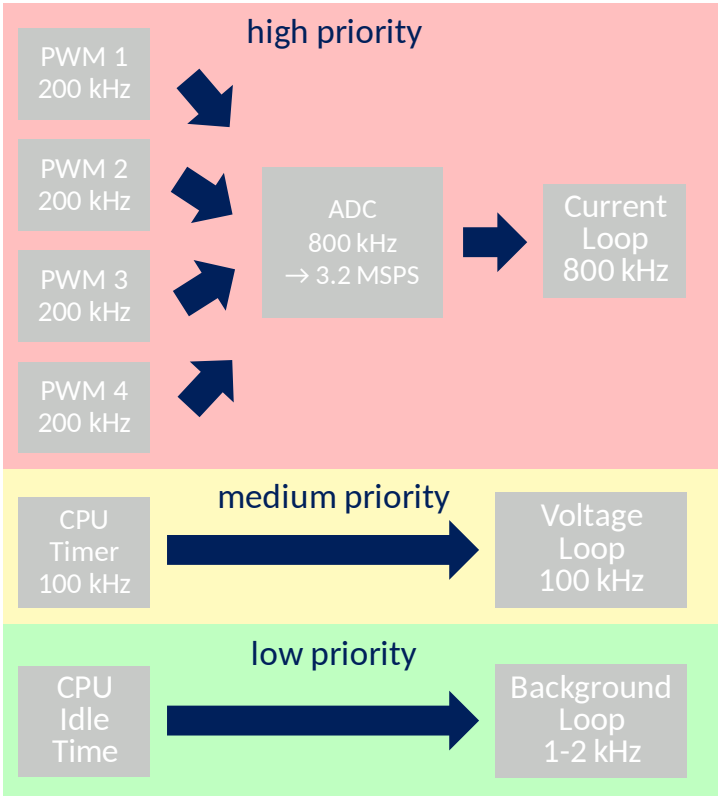


Figure 7.1: There are three different loop function priority levels with distinct execution rates.

This practice is not exact due to ISR and function call overheads and will result in a slightly shorter measured execution times compared to the real execution time. Figures 7.2 and 7.3 show screenshots of the used software PulseView to visualize the logic pin states with marked execution times and periods.

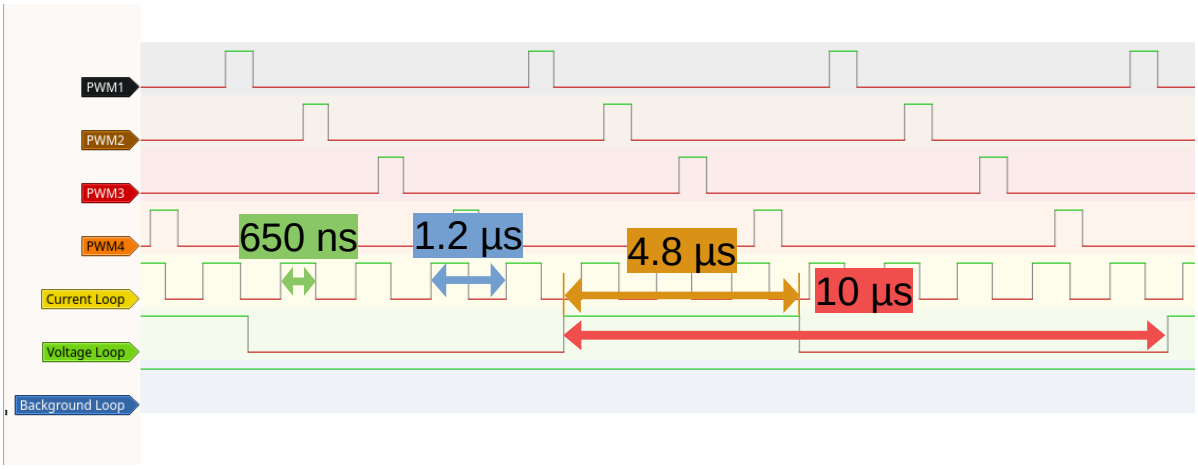


Figure 7.2: Capture of the execution times (green and orange marked) and execution period (blue and red marked) of the current loop and the voltage loop.

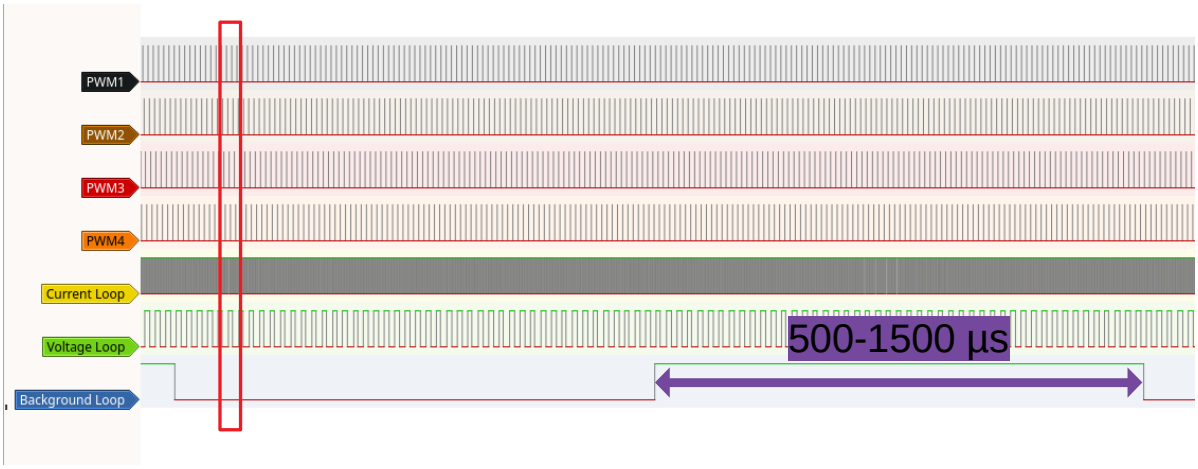


Figure 7.3: Capture of the execution time of the background loop (marked violet). The value is not fixed and depends on the CPU time used by the other loop functions as well as the use of the RFO. The red box corresponds to the time period shown in figure 7.2.

7.2.1 Current Loop Function

The current loop function's task is to perform the calculation of the current loop controller (see section 8.1) based on input data from the ADC and manipulating the duty cycle of the PWM generators.

In four rail mode the ADC trigger frequency is equal to the execution frequency of the current loop function. For the maximum frequency of 800 kHz this corresponds to a period time of 1.2 µs. This is the maximum allowed execution time for the current loop function including ISR overhead. To provide CPU time for the other two loops the execution time should be less than 1.2 µs. In this project a maximum current loop execution time excluding overhead of approx. 660 ns in debug build mode and 540 ns in release build mode is reached.

When the current loop function is triggered it has to be determined which rail the current measurements were taken from. Using an event flag of one PWM generator the originating rail can be determined every fourth function call. In between the originating rail can be determined using a counter, which involves using a chain of if statements or a switch statement. Both statements cause a jitter in the function execution time over four consecutive function calls, which is caused by a varying number of CPU instructions needed for a function run. This jitter results in a higher worst-case execution time for the current loop and needs to be reduced for increased stability.

To overcome this issue a linked list is used to keep track of the originating rail. The struct used in one linked list element contains pointers to ADC result registers and PWM compare registers for one particular rail. Only a single if statement is used to reset the linked list position or switch to the next linked list element. This approach has the further benefit of enabling a manual control mode by switching the linked list head to another linked list filled with dummy values without increasing the number of if statements in the current loop function.

7.2.2 Voltage Loop Function

The voltage loop function handles the calculation of the higher level voltage loop controller (see section 8.2), supervises and limits the input and output voltages and disables the PWM outputs if exceeded, performs the change of the number of active rails as well as the change of the PWM switching frequency and provides a voltage ramp at converter start or manual output voltage change. Furthermore, it provides the inverse of the measured input voltage used in the feed forward part of the current loop controller.

Normally the number of active rails and the switching frequency are determined in the background loop's rail frequency optimization (RFO). In case of a sudden current demand and if not all four rails are active at this moment the voltage loop function can override the RFO and decide to increase the number of active rails on its own. This ability is needed because the background loop has a response time in the 500 µs to 2000 µs range and is therefore not able to meet the timing requirements during a current surge.

Unlike the current loop function the voltage loop function is triggered at a constant rate of 100 kHz by a CPU timer [12, p. 81]. The fixed execution rate eases the PI controller implementation of the voltage loop controller, because the integration part factor K_{iu} can be kept constant.

During normal four rail converter operation with activated current loop the voltage loop function run completes in about 5 µs. This leaves approx. 20% of available CPU time for use in the background loop.

7.2.3 Background Loop Function

The background loop function utilizes the remaining CPU time to perform temperature monitoring of the converter, trip zone handling, optimization of the number of active rails and the switching frequency as well as setting the PWM duty cycle in manual mode.

The temperature sensor onboard the converter board is sampled every background

loop run and the median is calculated over 21 samples. Using the median value, the temperature is classified with hysteresis in three temperature levels cold, normal and overheating. The classification temperature limits are guessed and have to be adjusted during tests with the finished control board.

If the trip input of one PWM module is triggered, its output will be disabled in hardware and a hardware register flag is set. This flag will be read in the background loop and if it is set all PWM generators will be disabled in software and the hardware trip state will be lifted.

To achieve a higher converter efficiency the number of active rails and the switching frequency can be adjusted automatically during operation. This is done in a function of the RFO translation unit which will be called within the background loop. The RFO function will be provided with the values of the filtered current over all rails, the temperature and the input and output voltage. Using this input data, it calculates the optimal number of rails and the switching frequency to maximize the converter efficiency. Currently the RFO does not touch the converter frequency and is changing the number of active rails based on pre-defined current levels with hysteresis only.

7.3 Floating-Point Arithmetic

The TMS320C28x MCU family the F28335-MCU counts to possesses a floating-point unit which accelerates floating-point calculations in hardware [13]. During firmware development no maximum execution time difference for current loop function runs could be observed when implemented in integer arithmetic or in floating-point arithmetic.

Because of this observation it is chosen to perform all control loop calculations in floating-point arithmetic. The benefit of this approach is an easier to read code, because shifting operations and accuracy considerations of fixed-point math are omitted. During debug sessions the variable values can directly be interpreted without scale factor.

For the feed forward part of the current controller the inverse of the measured input

voltage is needed. Due to its computational complexity its calculation by division is not carried out in the current loop function, but in the voltage loop function. The F28335-MCU is able to calculate float divisions with 8 bits of accuracy in hardware [13, p. 51]. To achieve full 32-bit floating point accuracy, an approximation algorithm in software is used afterwards. The fastRTS library used in this project uses a Newton-Raphson algorithm to achieve this accuracy and is optimized in terms of speed for the TMS320C28x MCU family [14]. The library is not used by default in newly created projects in the integrated development environment (IDE) Code Composer Studio. It has to be added manually in the project settings.

7.4 Converter Control During Debug Sessions

To control the converter and test parameters during debug sessions a struct named `controlConfig` is used. It is declared in the file `control_loops.h`. To easily access its

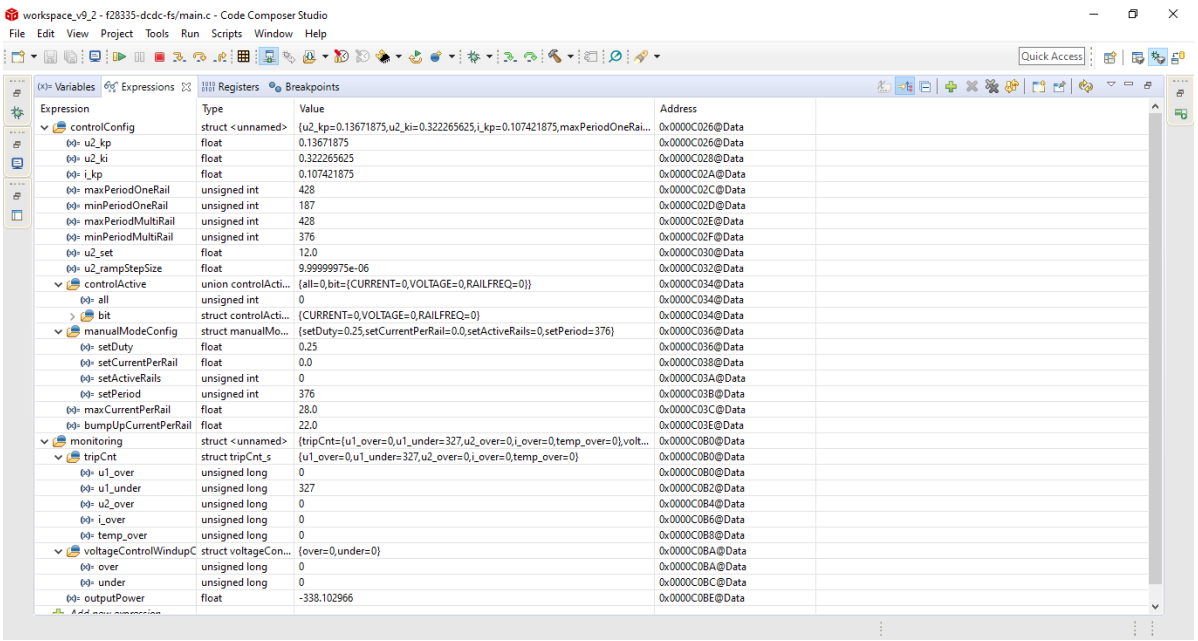


Figure 7.4: Screenshot of the IDE Code Composer Studio showing the variable watches used to control the converter during operation.

values a variable watch to this struct can be used as seen in figure 7.4 . When starting up the control card, its PWM outputs are disabled by default. The settings `CURRENT`, `VOLTAGE`, `RAILFREQ` at `controlConfig.controlActive.bit` are set to zero, this enables the manual mode for the current loop, the voltage loop and the RFO. Finally, all rails are disabled by setting `controlConfig.manualModeConfig.setActiveRails` to zero. This off-state is reentered if the PWM generator outputs are disabled in cause of temperature overshoot, voltage limit violation or a trip zone event as described in sections 7.2.2 and 7.2.3.

To disable the manual mode and enable the control loops all at once the setting `controlConfig.controlActive.all` is to be set to value 7. The initial setting values at control board startup are defined in the code block described as 'Initial values for setting structs' in the same file.

A second struct of interest resides in file `monitoring.h` and is named `monitoring`. Its purpose is to count failure event occurrences which lead to PWM output shutdowns in the nested struct `tripCnt`. The nested struct `voltageControlWindupCnt` also documents how often the anti-windup functionality of the voltage controller has reset the integral part. Finally, the current output power is given by the struct's value `outputPower`.

For further setting options, please refer to the documented source code.

7.5 Possible Improvements of the Firmware

To date the firmware was tested with a logic analyzer and manual set input pins connected to the control board. Due to the 2020 pandemic, the control board could not yet be tested in real operation with the newly developed converter board. Corresponding tests must still be carried out in the future.

If it turns out that debugging the control card using the JTAG-Interface while connected to the converter board is not possible due to electromagnetic interferences or isolation problems, the RS-232 interface pads located on the converter board could be

used to establish a more robust communication channel. The control board is equipped with a RS-232 level shifter MAX3221 and an ISO7221 digital isolator to provide a galvanic isolated RS-232 interface with $\pm 12\,\mathrm{V}$ signal levels [15].

The RFO implementation in file `rail_frequency_optimization.c` is simple and does not account for temperature and voltage measurements. The implementation could be improved by using a pre-trained neural network to find the operating point that leads to the highest converter efficiency (see [16]).

If three rails are active, the PWM phase distances are not equal. This could be addressed by changing the PWM phase settings before entering and leaving the triple rail mode in the voltage loop function.

8 Re-Dimensioning of Control

The topology used for controlling of this converter is an outer voltage control loop with an inner current control loop for each of the current rails. This type of control is thoroughly analyzed in [17] and its implementation for this converter is documented in [8]. While usage of the new F28335-Card does not influence the basic control structure, some parameters have to be adjusted to achieve the same closed-loop behavior as before.

8.1 Current Control-Loop

Most important change for the current control is the fact that the new F28335-Card cannot sample each rail's current twice per switching period because of its slower clock speed. Sampling the currents only once per switching period results in a sampling frequency that is only half as much as before.

The current controller is a simple proportional controller since a steady state error of zero is not required for the inner control-loop.

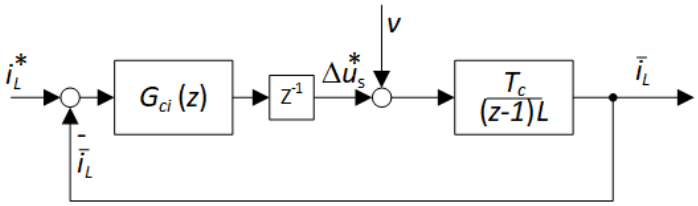


Figure 8.1: Current control loop [8].

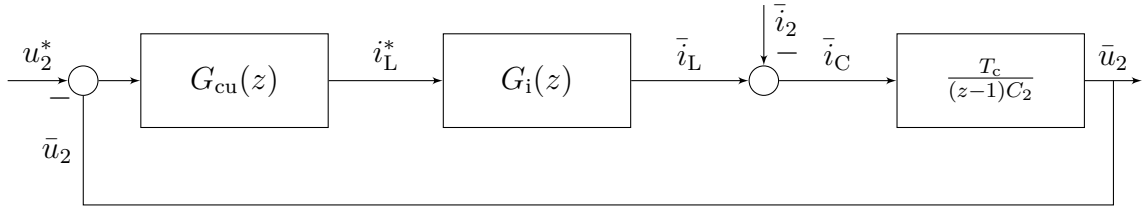


Figure 8.2: Voltage control loop based on [8] but with a correction on the capacitor's transfer function.

Based on results from [8] the current control loop is shown in figure 8.1 and its z-domain closed-loop transfer-function is given by

$$G_{\mathrm{i}}(z) = \frac{\frac{K_{\mathrm{pc}}T_{\mathrm{c}}}{L}}{z^2 - z + \frac{K_{\mathrm{c}}T_{\mathrm{pc}}}{L}} \tag{8.1}$$

with K_{pc} being the parameter of the proportional controller, T_{pc} being the sampling period of the current measurement and L being inductance of each rail's coil.

The parameter K_{pc} should be chosen in a way that prevents an overshoot of the currents in closed-loop control. According to [16] this is the case for

$$K_{\mathrm{pc}} = \frac{L}{4T_{\mathrm{c}}}. \tag{8.2}$$

It should again be noted that the relation between switching frequency and sampling period $f_{\mathrm{s}} = \frac{1}{T_{\mathrm{c}}}$ is chosen different here than in [16] because of the F28335-Card's lower clock speed.

8.2 Voltage Control-Loop

Since the output voltage should have a steady state error of zero, a PI-controller is used for the voltage control loop which is shown in figure 8.2. It can also be seen that because the voltage control is an outer loop it contains the current control loop as a plant.

Based on [8] (but correcting a minor mistake) the z-domain closed-loop transfer-

function for the voltage controller is given by

$$G_{\mathrm{u}}(z) = \frac{G_{\mathrm{cu}}(z)G_{\mathrm{i}}(z)\frac{T_{\mathrm{c}}}{(z-1)C_2}}{1 + G_{\mathrm{cu}}(z)G_{\mathrm{i}}(z)\frac{T_{\mathrm{c}}}{(z-1)C_2}} \tag{8.3}$$

where C_2 is the capacitance of the converter's output capacitor and

$$G_{\mathrm{cu}}(z) = K_{\mathrm{pu}} + K_{\mathrm{iu}}\frac{T_{\mathrm{C}}}{z-1} \tag{8.4}$$

the transfer function of the PI-controller with proportional factor K_{pu} and integral factor K_{iu}.

In [8] the voltage controller's parameters are not chosen analytically but through a PLECS simulation. Since the simulation models and data are not available to this project group this approach cannot be followed directly for choosing the new controller's parameters.

It can be shown from equation 8.3 assuming $L = \text{const.}$ and $C_2 = \text{const.}$ that the closed loop transfer function does not change with a different T_{c} as long as the conditions

$$K_{\mathrm{pc}}T_{\mathrm{c}} = \text{const. and } K_{\mathrm{pu}}T_{\mathrm{c}} = \text{const. and } K_{\mathrm{iu}}^2T_{\mathrm{c}}^2 = \text{const.} \tag{8.5}$$

are true. This also matches the result for the current controller when comparing equation 8.2 to the equation in [16].

The conditions in equation 8.5 give an approach for scaling the current and voltage controllers' parameters relative to the sampling period T_{c}. To validate this approach a Simulink simulation is done comparing the old control design with the F28379D-Launchpad to the new design with the F28335-Card which is using a sampling period T_{c} twice as long.

The Simulink model is shown in figure 8.3. It is based on the linearized average model of a single half-bridge as shown in [8] and contains a mixture of time-discrete and continuous blocks to properly simulate the interaction between the discrete controller and the continuous components of the converter. With this model the performance of

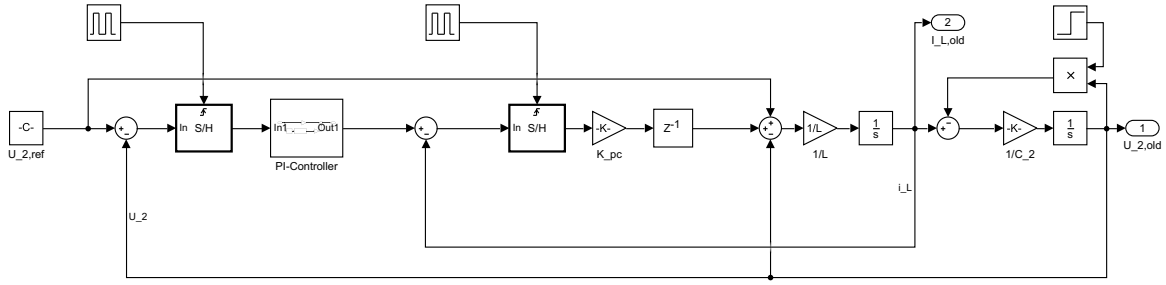


Figure 8.3: Simulink model for the control of one rail.

the old and new control are compared based on their behavior when applying a load jump from 0 W to 500 W. The old controller's parameters are directly taken from the code of the F28379D-Launchpad. The new controller's parameters are obtained through equation 8.2 for the current control loop. For the voltage control loop the new parameters are obtained by scaling the old parameters according to equation 8.5.

The simulation results are shown in figure 8.4. Especially the old control does not behave quite as expected showing a high current overshoot that should not be happening. This can be explained by the old current control's parameter K_{pc} actually not fulfilling equation 8.2 because it probably was hand-tuned based on simulations or measurements like the voltage control parameters. For this reason, the simulation results of the old and new control should not be compared directly to each other for now, since the new control tries to suppress current overshoots and is thus generally acting slower.

Since the new control is still reacting to the load jump reasonably fast its parameters are kept like in the simulation until testing on the real converter can be done. The approach of scaling control parameters according to equation 8.5 should also be kept in mind for future work where an alteration of the switching frequency might be done based on load conditions.

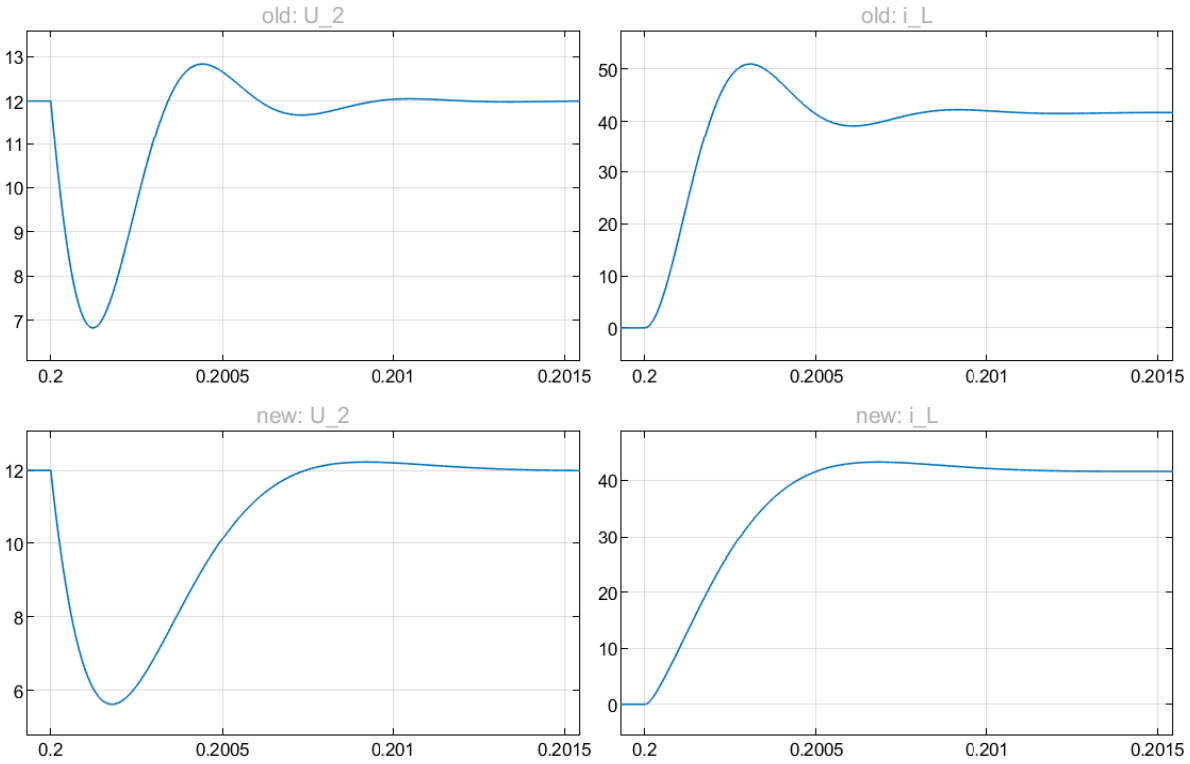


Figure 8.4: Results of the Simulink simulation comparing the old and new control's behavior when applying a load jump of 500 W.

9 Abstract

To increase the power density a 1 kW DC-DC Converter has been fully redesigned. Because of using a control card with small form factor but less computational power, the software architecture must take this lean environment into account. The code is comprehensively modified to achieve the best possible efficiency. Due to the requirements of one-sided input and output connectors the PCB layout is clearly separated in power traces and controlling signals. By a simulatively tested cooling strategy with bottom cooled GaN transistors, an adequate and robust connection of the PCB onto the water-cooled housing is implemented. Additionally, the water-proof housing concept completes the application-oriented and reasoned design.

The converter could not be put into operation because of the Corona Crisis in 2020. Although, during the process of developing extensive code documentation, many simulation results and CAD models have been created or renewed.

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